

CSMOSPEGM85M1

800G OSFP SR8 850 nm 100 m Transceiver Specification

Description

The CSMOSPEGM85M1 is an eight-channel parallel pluggable fiber-optic OSFP transceiver designed for 800 Gigabit Ethernet applications. This high-performance module is optimized for short-range data communication and interconnect applications, integrating eight 53.125 GBd PAM4 lanes in each direction. The maximum transmission distance is up to 60 m over OM3 MMF or 100 m over OM4 MMF. The module operates over multimode fiber systems using a nominal wavelength of 850 nm.

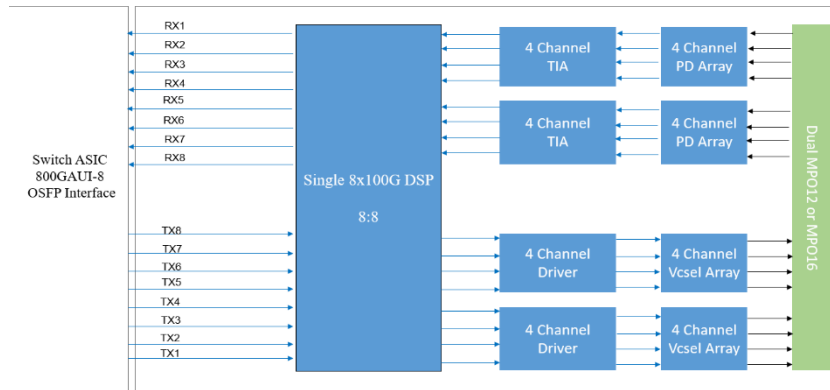
Features

- ◆ OSFP Serial Optical Interface
 - 8 × 100G PAM4 Retimed 800GAUI-8 Electrical Interface
 - Dual MPO-12 APC and MPO-16 APC Connectors
 - 8-Channel VCSEL Arrays and 8-Channel PIN Photodetector Arrays
 - Maximum Link Length of 60 m over OM3 MMF or 100 m over OM4 MMF
- ◆ OSFP MSA Compliant
 - Hot-Pluggable OSFP Form Factor
 - Compliant with OSFP Module Specification Rev. 5.0
 - Compliant with CMIS 5.2
- ◆ Supported Protocols
 - Compliant with IEEE 802.3db
 - Compliant with IEEE 802.3ck
- ◆ Low Power Consumption
 - Less Than 14 W over an Operating Case Temperature Range of 0 °C to +70 °C

Applications

- 800GBASE-SR8 Ethernet
- Data Center Networks

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Relative Humidity (Non-Condensing)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold per Lane	PRdmg	5		dBm

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Top	0	70	°C
Relative Humidity (Non-Condensing)	RH	15	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption	Pc		14	W
Module Supply Current			4.465	A
Bit Rate	BR		850	Gbps
Fiber Length on OM3 MMF			60	m
Fiber Length on OM4 MMF			100	m
2-Wire Serial Interface Clock Frequency	0		400	kHz

Notes:

Under conditions of 3.465 V operating supply voltage and +70 °C case temperature.

Optical Specifications

Parameter		Symbol	Min	Typical	Max	Unit
Transmitter						
Data Rate per Lane		DR		53.125		GBd
Modulation format			PAM4			
Center Wavelength ¹		λ	840	860	868	nm
RMS spectral width		σ			0.6	nm
Average Launch Power, Each Lane		Pavg	-4.6		4	dBm
Optical Power OMA, Each Lane, Max.			3.5			dBm
OMAouter, each lane min	max (TECQ, TDECQ) < 1.8 dB 1.8 < max (TECQ, TDECQ) < 4.4 dB	POMA	max [-2.6, max(TECQ, TDECQ) – 4.4]			dBm
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), Each Lane		TDECQ			4.4	dB
Transmitter Eye Closure for PAM4 (TECQ), Each Lane		TECQ			4.4	dB
Extinction Ratio		ER	2.5			dB
Transmitter Power Excursion, Each Lane					2.3	dBm
Optical Return Loss Tolerance		ORLT			14	dB
Optical Power for TX Disable					-30	dBm
Encircled Flux ²			≥ 86 % at 19 ≤ 30 % at 4.5			μm
Receiver						
Data Rate per Lane		BR		53.125		GBd
Modulation format			PAM4			
Center Wavelength		λ	842	850	948	nm
Damage Threshold			5			dBm
Average Receive Power, Each Lane			–6.4		4	dBm
Receive Power, Each Lane (OMAouter)					3.5	dBm
Receiver Reflectance		Rr			–15	dB
Receiver Sensitivity, Each Lane ³			RS = max(-4.6, TECQ – 6.4)			dBm
Stressed Receiver Sensitivity, Each Lane					–2	dBm
LOS Assert			-15			dBm
LOS De-Assert					-7.5	dBm
LOS Hysteresis			0.5		5	dB

Notes:

1. Defined according to the performance of the laser used.
2. Measured into type A1a.2, A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.
3. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Electrical Specifications

Parameter	Min	Typical	Max	Unit
Pre FEC Bit Error Ratio			2.40E-04	
Post FEC Bit Error Ratio			1.00E-12	
Transmitter, Each Lane				
Differential Peak-to-Peak Input Voltage Tolerance	750			mV
Differential Termination Mismatch			10	%
Eye Height	10			mV
Common-Mode to Differential-Mode Return Loss	IEEE 802.3ck Equation (120G–1)			dB
Vertical Eye Closure			12	dB
Effective Return Loss	7.3			dB
Transition Time	10			ps
Receiver, Each Lane				
Differential Data Output Swing	300		900	mVpp
Differential Termination Mismatch			10	%
Eye Height	15			mV
Vertical Eye Closure			12	dB
Common-Mode to Differential-Mode Return Loss	IEEE 802.3ck Equation (120G–1)			dB
Effective Return Loss	8.5			dB
Transition Time	8.5			ps

Software and Management Features

➤ Management Interface

The CSMOSPEGM85M1 transceiver is compliant with the OSFP Module Specification Rev. 5.0 and the Common Management Interface Specification (CMIS) Rev. 5.2. It provides a 2-wire serial management interface for module monitoring, configuration, and control.

➤ Supported Application Modes

The transceiver supports flexible multi-rate application modes through standard CMIS mechanisms. Supported application modes and breakout configurations include:

- 800G Ethernet: 800GBASE-SR8
- 400G Ethernet: 400GBASE-SR8 and 2 × 400GBASE-SR4
- 200G Ethernet: 200GBASE-SR8 and 4 × 200GBASE-SR2
- 100G Ethernet: 8 × 100GBASE-SR1 breakout modes

Detailed application selection and configuration procedures are available upon request.

➤ **Diagnostic and Control Features**

To support robust link performance and simplify system-level troubleshooting, the module provides the following diagnostic and signal control features:

- TX and RX Squelch Functions
- TX Adaptive Input Equalization
- RX Output Equalization
- RX Output Amplitude Control
- Host-Side and Media-Side Loopback Capabilities on a Per-Lane Basis

➤ **Digital Diagnostic Monitor Accuracy**

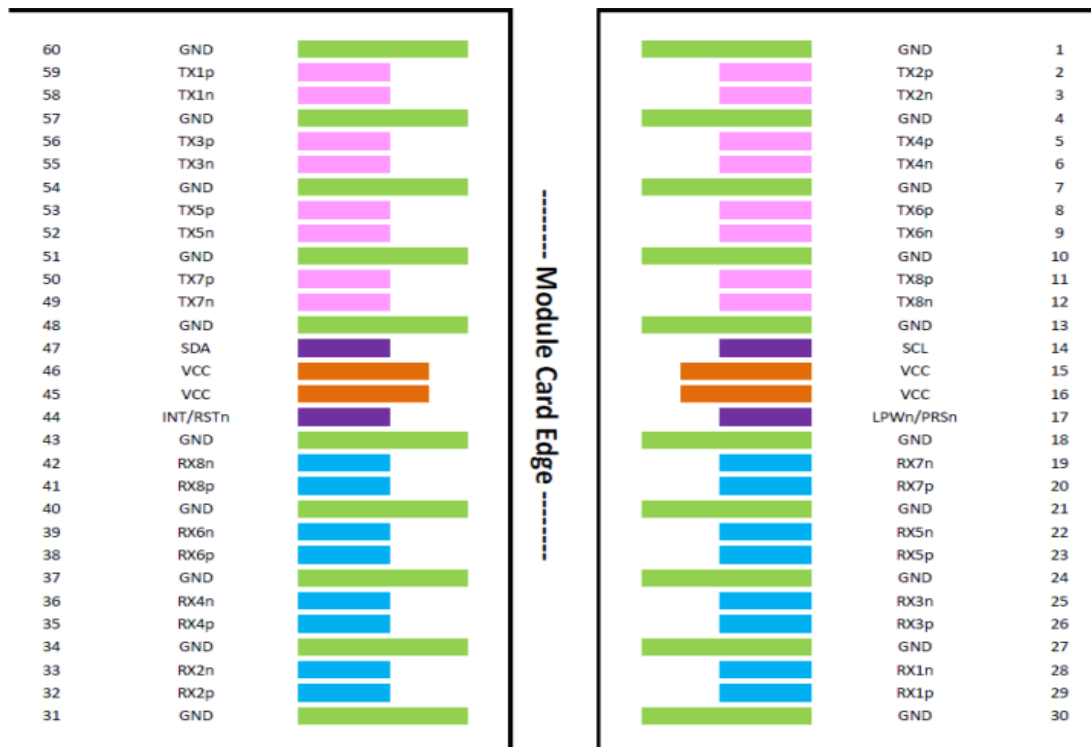
The transceiver supports real-time monitoring of key operating parameters. The digital diagnostic monitoring accuracy is defined over the recommended operating conditions.

Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	±3	°C
Internally Measured Transceiver Supply Voltage	±3	%
Measured TX Bias Current	±10	%
Measured TX Output Power	±3	dB
Measured RX Received Average Optical Power	±3	dB

Notes:

1. The temperature test point is located at the specified hotspot of the module.
2. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reports -40 dBm when the transmitter is disabled.

Pin Diagram



Pin Definitions

Pin	Name	Logic	Description	Plug Seq.	Notes
1	GND		Ground	1	
2	TX2p	CML-I	Transmitter Data Non-Inverted	3	
3	TX2n	CML-I	Transmitter Data Inverted	3	
4	GND		Ground	1	
5	TX4p	CML-I	Transmitter Data Non-Inverted	3	
6	TX4n	CML-I	Transmitter Data Inverted	3	
7	GND		Ground	1	
8	TX6p	CML-I	Transmitter Data Non-Inverted	3	
9	TX6n	CML-I	Transmitter Data Inverted	3	
10	GND		Ground	1	
11	TX8p	CML-I	Transmitter Data Non-Inverted	3	
12	TX8n	CML-I	Transmitter Data Inverted	3	
13	GND		Ground	1	
14	SCL	LVCMOS-I/O	2-Wire Serial Interface Clock	3	
15	VCC		+3.3 V Power	2	
16	VCC		+3.3 V Power	2	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	3	1A
18	GND		Ground	1	

19	RX7n	CML-O	Receiver Data Inverted	3	
20	RX7p	CML-O	Receiver Data Non-Inverted	3	
21	GND		Ground	1	
22	RX5n	CML-O	Receiver Data Inverted	3	
23	RX5p	CML-O	Receiver Data Non-Inverted	3	
24	GND		Ground	1	
25	RX3n	CML-O	Receiver Data Inverted	3	
26	RX3p	CML-O	Receiver Data Non-Inverted	3	
27	GND		Ground	1	
28	RX1n	CML-O	Receiver Data Inverted	3	
29	RX1p	CML-O	Receiver Data Non-Inverted	3	
30	GND		Ground	1	
31	GND		Ground	1	
32	RX2p	CML-O	Receiver Data Non-Inverted	3	
33	RX2n	CML-O	Receiver Data Inverted	3	
34	GND		Ground	1	
35	RX4p	CML-O	Receiver Data Non-Inverted	3	
36	RX4n	CML-O	Receiver Data Inverted	3	
37	GND		Ground	1	
38	RX6p	CML-O	Receiver Data Non-Inverted	3	
39	RX6n	CML-O	Receiver Data Inverted	3	
40	GND		Ground	1	
41	RX8p	CML-O	Receiver Data Non-Inverted	3	
42	RX8n	CML-O	Receiver Data Inverted	3	
43	GND		Ground	1	
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	3	1B
45	VCC		+3.3 V Power	2	
46	VCC		+3.3 V Power	2	
47	SDA	LVC MOS-I/O	2-Wire Serial Interface Data	3	
48	GND		Ground	1	
49	TX7n	CML-I	Transmitter Data Inverted	3	
50	TX7p	CML-I	Transmitter Data Non-Inverted	3	
51	GND		Ground	1	
52	TX5n	CML-I	Transmitter Data Inverted	3	
53	TX5p	CML-I	Transmitter Data Non-Inverted	3	
54	GND		Ground	1	
55	TX3n	CML-I	Transmitter Data Inverted	3	
56	TX3p	CML-I	Transmitter Data Non-Inverted	3	
57	GND		Ground	1	
58	TX1n	CML-I	Transmitter Data Inverted	3	

59	TX1p	CML-I	Transmitter Data Non-Inverted	3	
60	GND		Ground	1	

Notes:

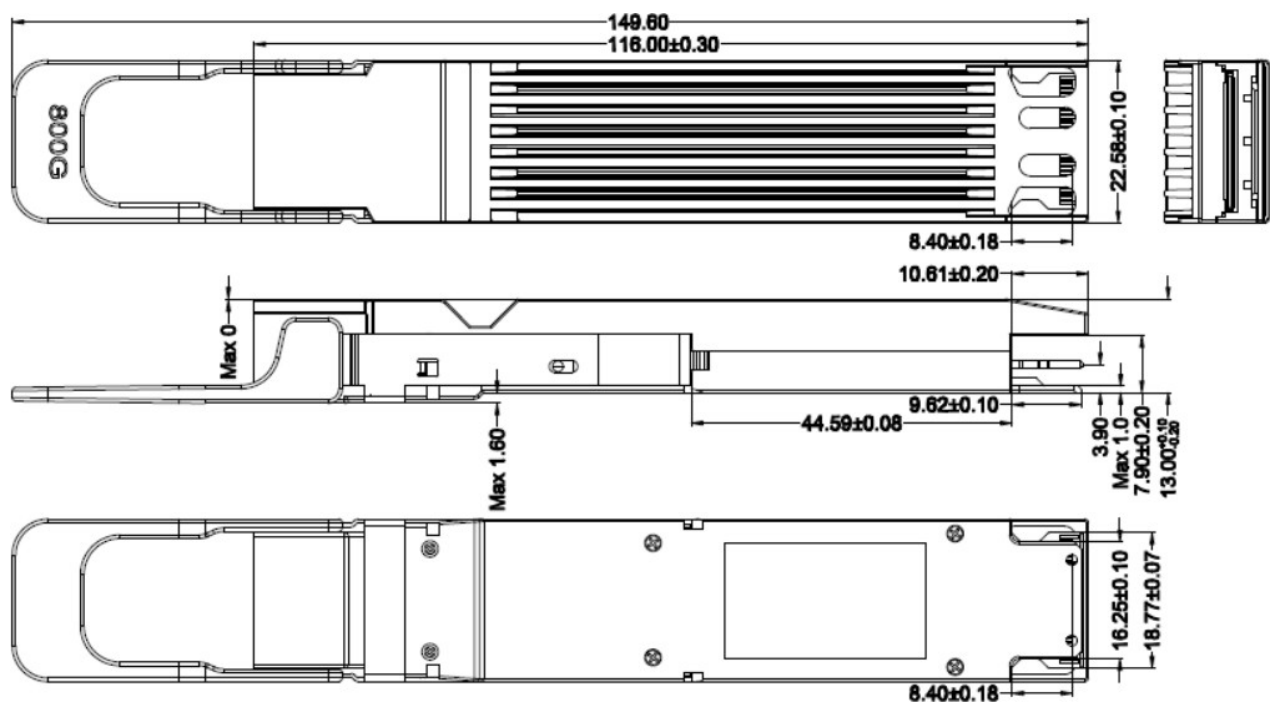
1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1, 2, 3.
2. LPWn/PRSn is a multi-level signal for low-power control from the host to the module and module presence indication from the module to the host. It is designed according to Section 13.5.3 of the OSFP Module Specification.
3. INT/RSTn is a multi-level signal for interrupt request from the module to the host and reset control from the host to the module. It is designed according to Section 13.5.2 of the OSFP Module Specification.

Mechanical Dimensions

Package Dimensions

The following figure shows the package dimensions of the module.

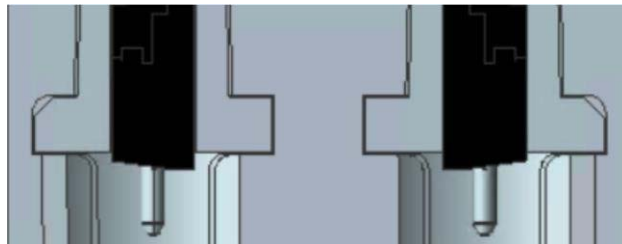
Package dimensions are specified in OSFP MSA.



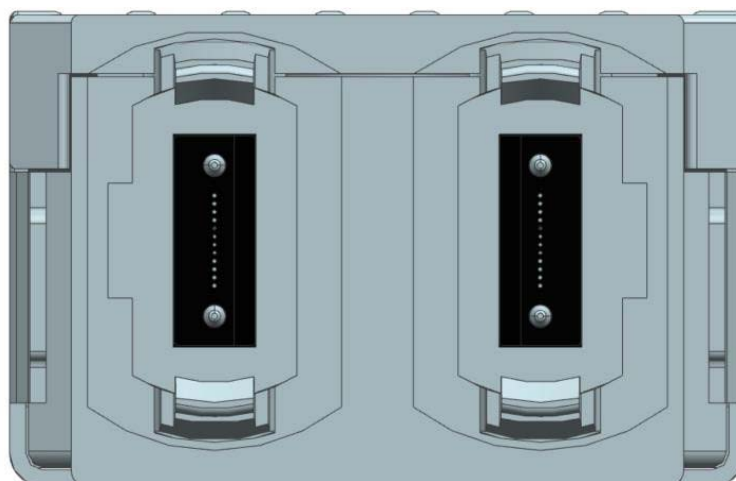
Unit: mm

Pull-Tab Color and Module Appearance

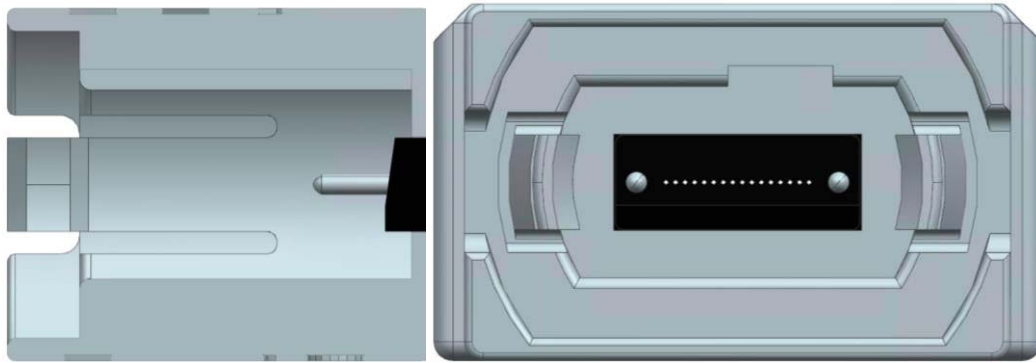
Dual MPO-12 Module with Pantone 475U (Beige) Pull-Tab

**Optical Interface Requirements**

MPO-16 Module Appearance



Dual MPO-12 APC Interface



The optical port provides two options: Dual MPO-12 APC and MPO-16 APC.

Ordering Information

Part Number	Product Description
CSMOSPEGM85M1D	800 Gbps, OSFP SR8, 850 nm, 100 m, Dual MPO-12, 0 °C to +70 °C
CSMOSPEGM85M1B	800 Gbps, OSFP SR8, 850 nm, 100 m, MPO-16, 0 °C to +70 °C

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