CSMOSPEGS31S5

800G OSFP DR8 1311 nm 500 m Transceiver Specification

Description

The CSMOSPEGS31S5 is an 800G OSFP DR8 transceiver module designed for 500 m optical communication applications over single-mode fiber. It is compliant with the OSFP MSA and applicable IEEE 802.3 standards. Powered by a silicon photonics (SiPh) platform, this transceiver integrates active and passive optoelectronic components, 3D packaging technology, and a 7 nm DSP. The module is designed for operation in data center environments and supports operation over the specified temperature and humidity ranges. Management and configuration features are accessible via a 2-wire serial interface.

Features

- Compliant with OSFP MSA and CMIS
- 8 × 106.25 Gbps (53.125 GBd PAM4) Electrical Interface
- 8 × 106.25 Gbps (53.125 GBd PAM4) Optical Architecture
- Power Consumption Less Than 16 W
- Maximum Link Length of 500 m over G.652 SMF with KP-FEC
- Dual MPO-16 APC Receptacles
- Built-In Digital Diagnostic Monitoring Functions
- Operating Case Temperature: 0 °C to +70 °C
- 3.3 V Power Supply Voltage
- RoHS Compliant

Applications

- 800GBASE-DR8
- Data Center Networks

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Maximum Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc + 0.3	V
Storage Temperature	Tst	-40	85	°C
Operating Case Temperature	Top	0	70	°C
Relative Humidity (Non-Condensing)	RH	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tca	0		70	°C
Data Rate per Lane	fd		53.125		GBd
Relative Humidity (Non-Condensing)	RH	5		85	%
Total Power Consumption	Pm			16	W

Optical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Center Wavelength	λc	1304.5		1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, Each Lane	Pout	-2.9		4	dBm	
Optical Modulation Amplitude (OMAouter), Each Lane	OMA	-0.8		4.2	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5		-	dB	
Average Launch Power of OFF Transmitter, Each Lane				-16	dBm	

Receiver						
Center Wavelength	λc	1304.5		1317.5	nm	
Receiver Sensitivity, OMAouter	RXsen			-4.4	dBm	1
Average Power at Receiver Input, Each Lane	Pin	-5.9		4	dBm	
Receiver Reflectance				-26	dB	
LOS Assert		-25			dBm	
LOS De-Assert				-6	dBm	
LOS Hysteresis		0.5			dB	

Notes：

1. Measured with a conformance test signal at TP3 for BER = 2.4E-4, Pre-FEC.

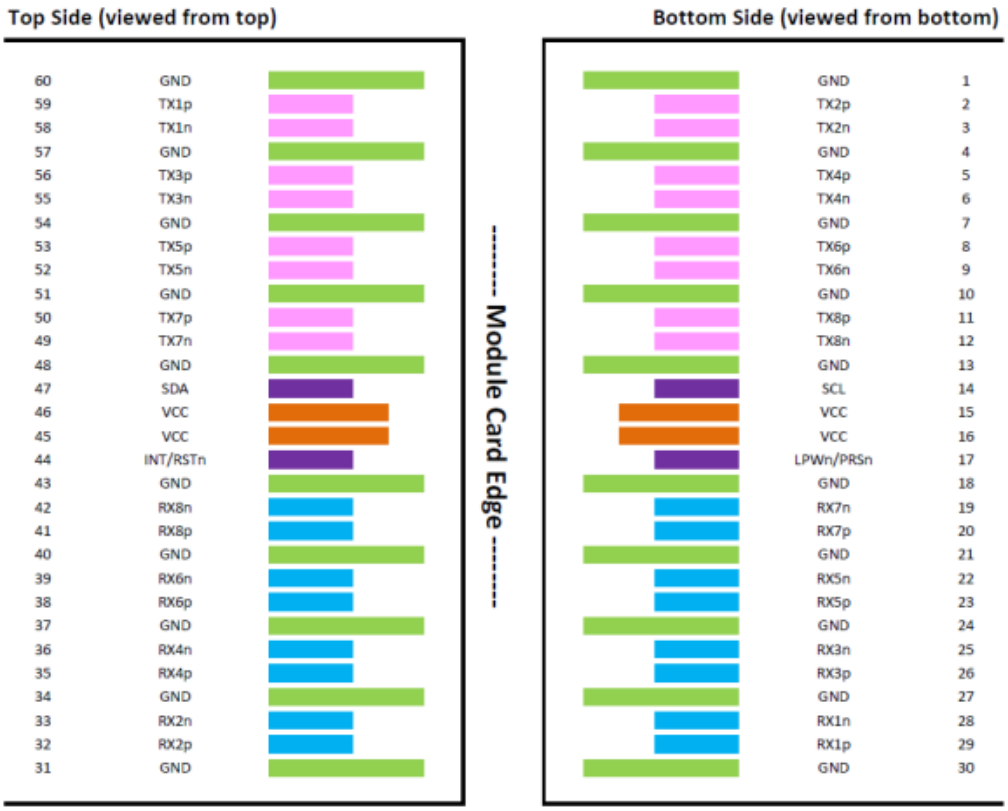
Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Zin	90	100	110	Ohm
Differential Output Impedance	Zout	90	100	110	Ohm
Differential Input Voltage Amplitude	ΔVin	400		900	mVp-p
Differential Output Voltage Amplitude	ΔVout			850	mVp-p
Bit Error Rate	BER			2.40E-04	
Input Logic Level High	VIH	2		Vcc	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	Vcc - 0.5		Vcc	V
Output Logic Level Low	VOL	0		0.4	V

Notes:

BER = 2.4E-4; PRBS31Q at 53.125 GBd, Pre-FEC.

Pin Diagram



OSFP Pinout

INT/RSTn

INT/RSTn is a dual-function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The circuit shown in Figure 1 enables multi-level signaling for bidirectional direct control. An active-low reset on the host is translated to an active-low reset on the module, while an active-high interrupt on the module is translated to an active-high interrupt on the host. The INT/RSTn signal operates across three voltage zones to indicate the module reset state and the host interrupt state, as shown in Figure 2. The host uses a 2.5 V reference to determine the H_INT state, and the module uses a 1.25 V reference to determine the M_RSTn state.

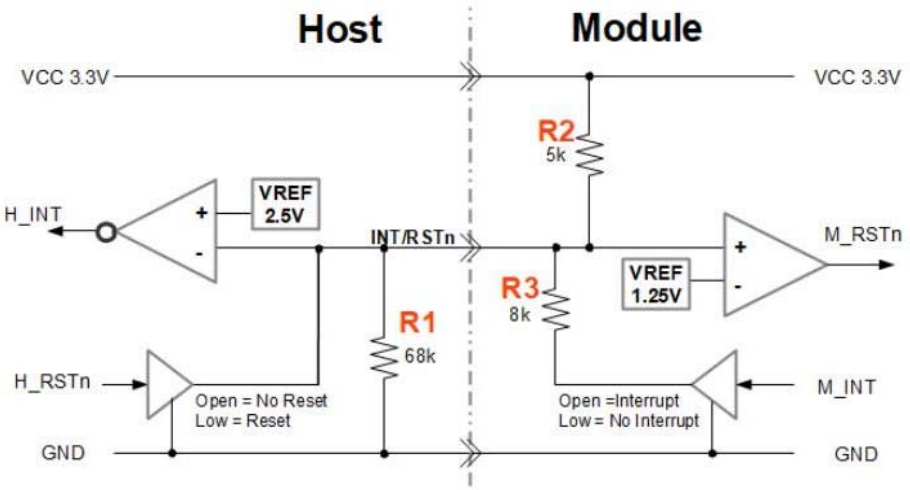


Figure 1

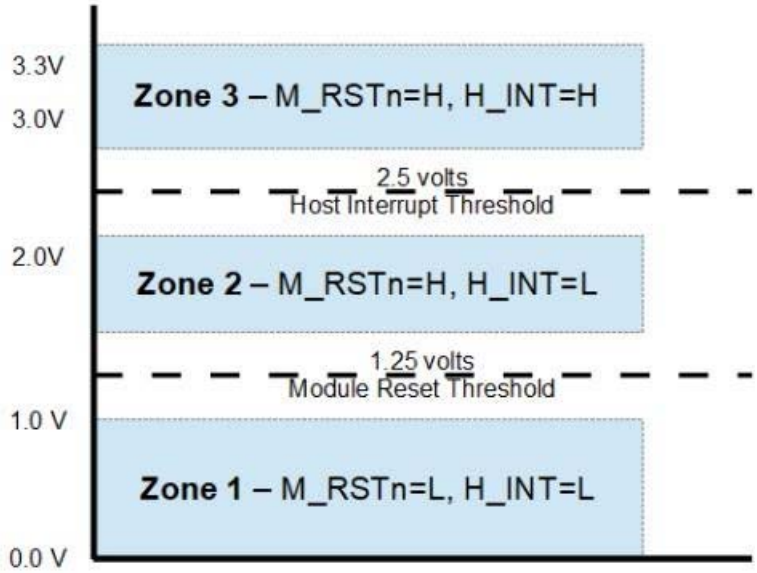


Figure 2

Zone 1 – Reset Operation – Zone 1 is the state when the module is in reset and the interrupt is deasserted (M_RSTn = Low, H_INT = Low). The min/max voltages for Zone 1 are defined by parameters V_INT/RSTn_1 and V_INT/RSTn_2 in Figure 3.

Zone 2 – Normal Operation – Zone 2 is the normal operating state with reset deasserted (M_RSTn = High) and interrupt deasserted (H_INT = Low). The min/max voltages for Zone 2 are defined by parameter V_INT/RSTn_3 in Figure 3.

Zone 3 – Interrupt Operation – In Zone 3, the module asserts an interrupt and must be out of reset (M_RSTn = High, H_INT = High). The min/max voltages for Zone 3 are defined by parameter V_INT/RSTn_4 in Figure 3.

Parameter	Nominal	Min	Max	Unit	Note
Host VCC	3.300	3.135	3.465	V	VCC voltage on the host
H_Vref_INT	2.500	2.475	2.525	V	Precision voltage reference for H_INT
M_Vref_RSTn	1.250	1.238	1.263	V	Precision voltage reference for M_RSTn
R1	68	66	70	kOhm	Recommended 68.1 kOhm, 1% resistor
R2	5	4.9	5.1	kOhm	Recommended 4.99 kOhm, 1% resistor
R3	8	7.8	8.2	kOhm	Recommended 8.06 kOhm, 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	V	INT/RSTn voltage for no module
V_INT/RSTn_2	0.000	0.000	1.000	V	INT/RSTn voltage for module installed, H_RSTn = Low
V_INT/RSTn_3	1.900	1.500	2.250	V	INT/RSTn voltage for module installed, H_RSTn = High, M_INT = Low
V_INT/RSTn_4	3.000	2.750	3.465	V	INT/RSTn voltage for module installed, H_RSTn = High, M_INT = High

Figure 3

LPWn/PRSn

LPWn/PRSn is a dual-function signal that allows the host to control Low Power Mode and allows the module to indicate Module Present. The circuit shown in Figure 4 enables multi-level signaling to provide direct signal control in both directions. Low Power Mode is an active-low signal on the host, which is converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module, which is converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in three voltage zones to indicate the state of Low Power Mode for the module and Module Present for the host. Figure 5 shows these three zones. The host uses a voltage reference at 2.5 V to determine the state of the H_PRSn signal, and the module uses a voltage reference at 1.25 V to determine the state of the M_LPWn signal.

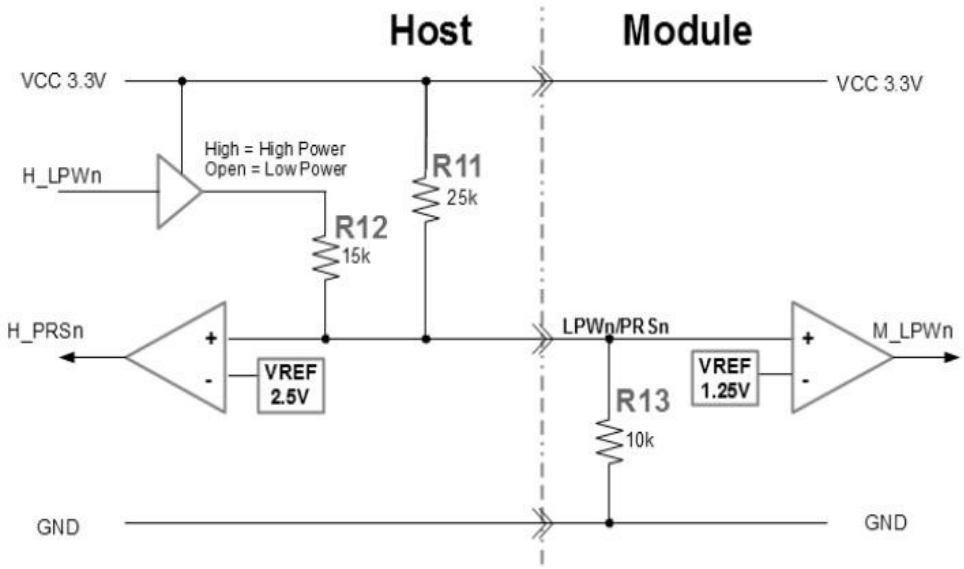


Figure 4

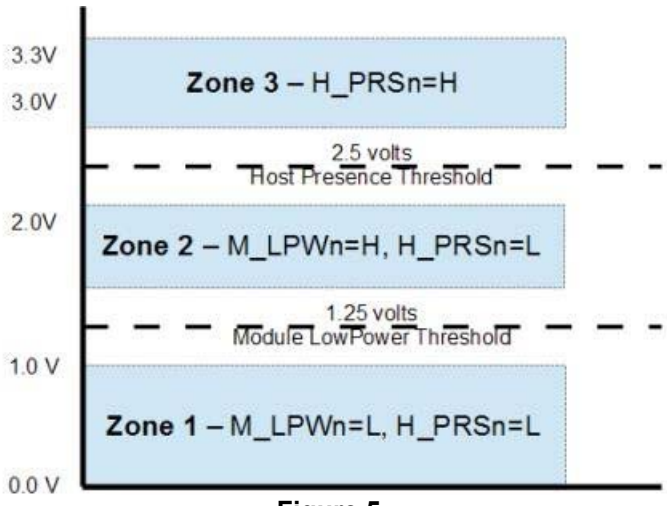


Figure 5

Zone 1 – Low-Power Mode – Zone 1 is the low-power state, and the module is present (M_LPWn = Low, H_PRSn = Low). The min/max voltages for Zone 1 are defined by parameter V_LPWn/PRSn_1 in Figure 6.

Zone 2 – High-Power Mode – Zone 2 is the high-power state, and the module is present (M_LPWn = High, H_PRSn = Low). The min/max voltages for Zone 2 are defined by parameter V_LPWn/PRSn_2 in Figure 6.

Zone 3 – Module Not Present – Zone 3 is the state in which the module is not present (H_PRSn = High). The min/max voltages for Zone 3 are defined by parameter V_LPWn/PRSn_3 in Figure 6.

Parameter	Nominal	Min	Max	Unit	Note
Host VCC	3.300	3.135	3.465	V	VCC voltage on the host
H_Vref_PRSn	2.500	2.475	2.525	V	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	V	Precision voltage reference for M_LPWn
R11	25	24.5	25.5	kOhm	Recommended 24.9 kOhm, 1 % resistor
R12	15	14.7	15.3	kOhm	Recommended 15 kOhm, 1 % resistor
R13	10	9.8	10.2	kOhm	Recommended 10 kOhm, 1 % resistor
V_LPWn/PRSn_1	0.950	0.000	1.100	V	LPWn/PRSn voltage for module installed, H_LPWn = Low
V_LPWn/PRSn_2	1.700	1.400	2.250	V	LPWn/PRSn voltage for module installed, H_LPWn = High
V_LPWn/PRSn_3	3.300	2.750	3.465	V	LPWn/PRSn voltage for no module

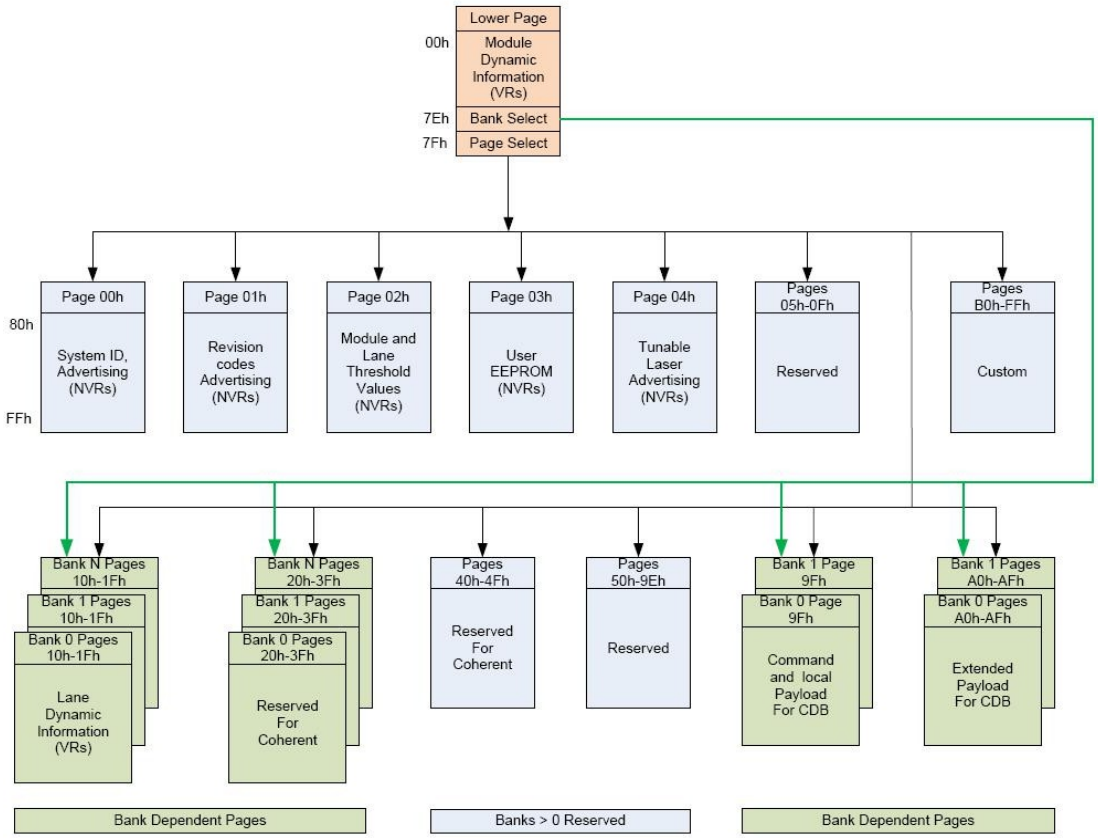
Figure 6

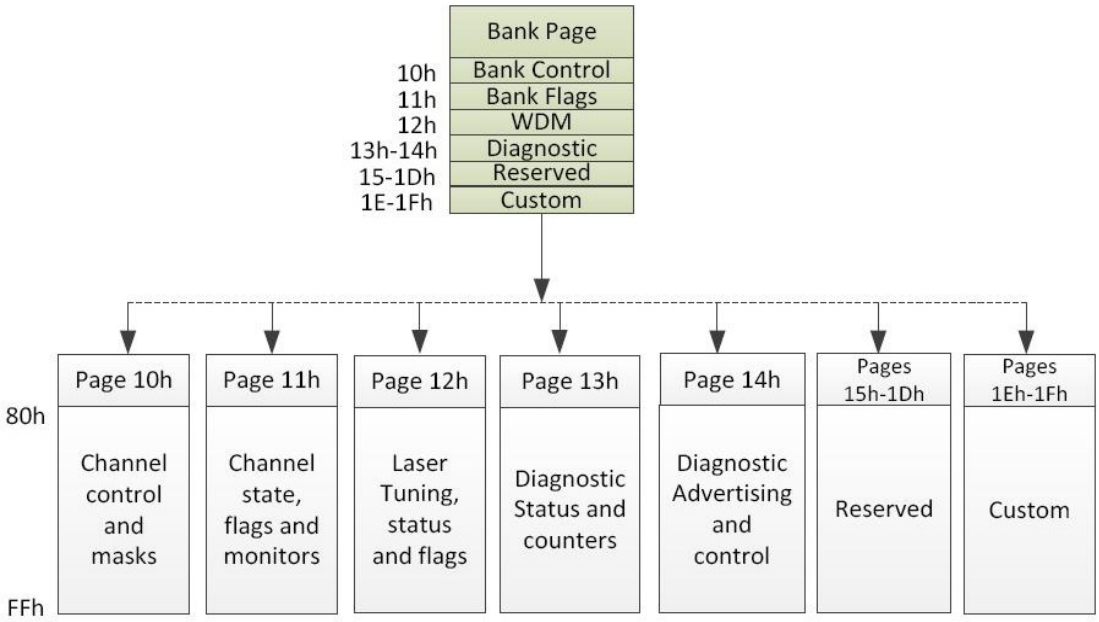
Pin Definitions

Pin	Symbol	Description	Logic	Direction	Plug Seq.	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-Wire Serial Interface Clock	LVCMOS-I/O	Bidirectional	3	Open-Drain with Pull-Up Resistor on Host
15	VCC	+3.3 V Power		Power from Host	2	
16	VCC	+3.3 V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bidirectional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	

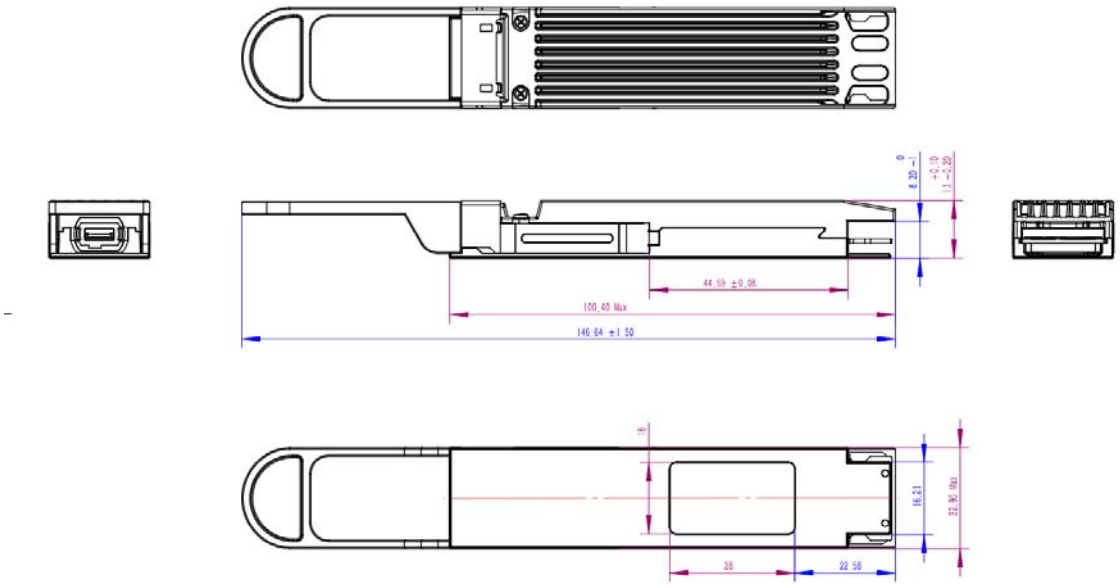
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bidirectional	3	See pin description for required circuit
45	VCC	+3.3 V Power		Power from Host	2	
46	VCC	+3.3 V Power		Power from Host	2	
47	SDA	2-Wire Serial Interface Data	LVCMOS-I/O	Bidirectional	3	Open-Drain with Pull-Up Resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Memory Map





Mechanical Dimensions



Unit: mm

Ordering Information

Part Number	Product Description
CSMOSPEGS31S5	800 Gbps, OSFP DR8, 1311 nm, 500 m, Dual MPO-16 APC, 0 °C to +70 °C

For More Information

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