CSMQ28HGL3140

100 Gbps QSFP28 Transceiver, Single-Mode, 40 km Reach

Description

The CSMQ28HGL3140 is a 100 Gb/s QSFP28 ER4 transceiver compliant with the QSFP28 MSA and IEEE 802.3ba. It is designed for use in 100 Gigabit Ethernet interfaces over single-mode fiber.

Features

- Hot-pluggable QSFP28 form factor
- Supports 103.1 Gb/s Aggregate Bit Rate
- Maximum Link Length of 40 km over Single-Mode Fiber (SMF)
- Power Dissipation < 5 W
- Built-In Digital Diagnostic Functions
- Built-in CDR
- 4 × 25.78 Gb/s DFB-Based LAN-WDM Transmitter
- Duplex LC Receptacles
- Single 3.3 V Power Supply
- RoHS Compliant
- Operating Case Temperature: 0 °C to +70 °C

Applications

- 100GBASE-ER4 Ethernet
- 100GE 4WDM-40

Absolute Maximum Ratings (Tc = 25 °C, Unless Otherwise Noted)

Module performance is not guaranteed beyond the operating range.
Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	Ts	-40		+85	°C	
Maximum Supply Voltage	Vcc	-0.3		3.6	V	
Operating Relative Humidity	RH	15		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Data Rate	DR	25.78 ± 100 ppm			Gb/s	1
Operating Case Temperature	Tc	0		70	°C	
Fiber Length over SMF	L			40	km	With FEC

Notes:

1. Supports 100GBASE-ER4 per IEEE 802.3ba.

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V_{CC}	3.135		3.465	V	
Supply Current	I_{CC}			1.5	A	
Module Total Power	P			5	W	1
Transmitter						
Signaling Rate per Lane		25.78 ± 100 ppm			Gb/s	
Differential Input Impedance	Zin		100		Ohm	
Differential Input Voltage Amplitude	Vin			900	mVp-p	
Receiver						
Signaling rate per lane		25.78 ± 100 ppm			Gb/s	
Differential Output Impedance	Z_{OUT}		100		Ohm	
Differential Output Voltage Amplitude	V_{OUT}	400		900	mVp-p	
Eye Width		0.57			UI	
Vertical Eye Closure				5.5	dB	
Transition Time, 20% to 80%	Tr/Tf	12			ps	

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.

Optical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Signaling Rate per Lane		25.78125 ± 100 ppm			Gb/s	1
Center Wavelength	λ	1294.53 – 1296.59 1299.02 – 1301.09 1303.54 – 1305.63 1308.09 – 1310.19			nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Transmit OMA per Lane	TXP	0.5		6.5	dBm	
Transmit Average Power per Lane	Pout	-2.5		6.5	dBm	
Optical Extinction Ratio	ER	4			dB	
Average Launch Power of OFF Transmitter, per Lane				-30	dBm	
Optical Return Loss Tolerance	RL			20	dB	
Relative Intensity Noise	RIN			-130	dB/Hz	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				2
Receiver						
Signaling Rate per Lane		25.78125 ± 100 ppm			Gb/s	1
Center Wavelength	λ	1294.53 – 1296.59 1299.02 – 1301.09 1303.54 – 1305.63 1308.09 – 1310.19			nm	
Average Receive Power per Lane	RXP	-20		-4	dBm	3
Receive Power (OMA) per Lane	RxOMA			-3.5	dBm	
Receive Sensitivity in OMA, each Lane	SEN			-18.5	dBm	4
Receiver Reflectance	Rfl			-26	dB	
LOS De-Assert	LOSD			-23	dBm	
LOS Assert	LOSA	-35			dBm	
LOS Hysteresis	LOSh	0.5			dB	

Notes:

1. The transmitter and receiver consist of four lasers and four photodiodes, with each channel operating at 25.78 Gb/s for 100GBASE-ER4.
2. BER ≤ 5E-5.
3. Average receive power, each lane (min), is informative and is not the principal indicator of signal

strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance..

4. Receiver sensitivity (OMA), each lane (max), at BER ≤ 5E-5 is a normative specification.

Pin Diagram

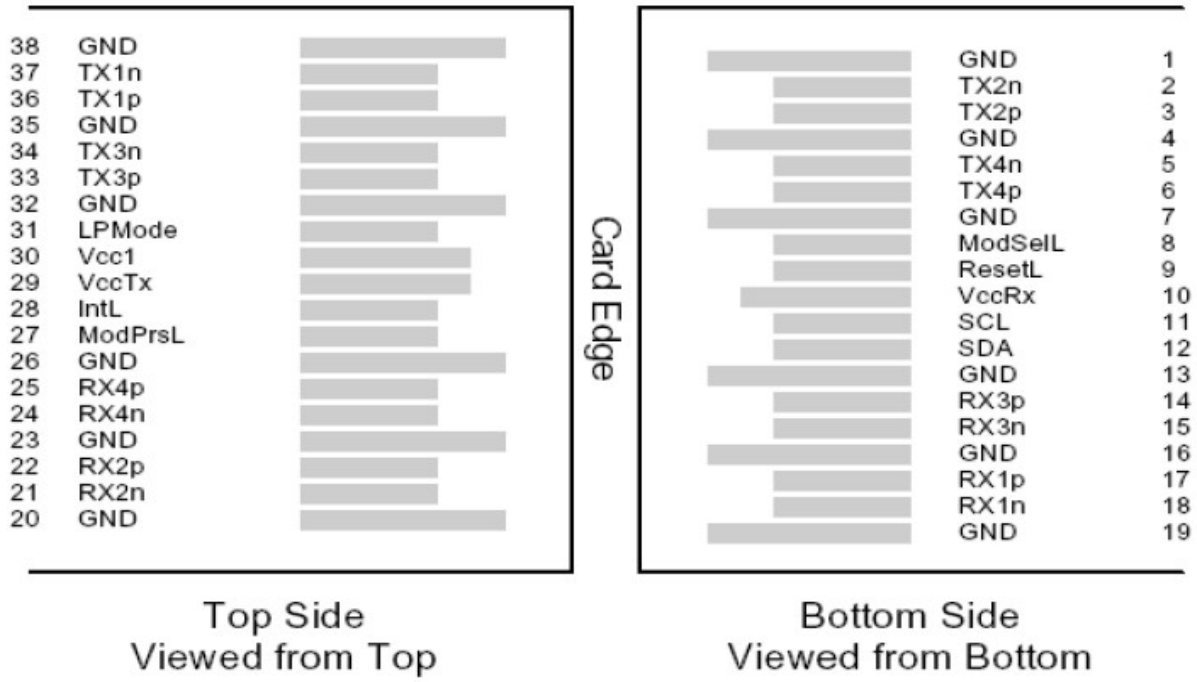


Figure 1 – QSFP28-Compliant 38-Pin Connector (per SFF-8679)

Pin Definitions

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	+3.3 V Power Supply Receiver	
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	

13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	2
29	VccTx	+3.3 V Power Supply Transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

1. Circuit ground is internally isolated from chassis ground.
2. IntL is an open-collector/drain output that should be pulled up with a 4.7 kOhm to 10 kOhm resistor on the host board. The IntL pin is deasserted High after completion of reset, once Byte 2, Bit 0 (Data_Not_Ready) is read as 0 and the flag field has been cleared (see SFF-8636).

Digital Diagnostic Functions

2-Wire Serial Address 1010000x
Lower Page 00h
0 Identifier
1- 2 Status
3- 21 Interrupt Flags
22- 33 Free Side Device Monitors
34- 81 Channel Monitors
82- 85 Reserved
86- 98 Control
99 Reserved
100-104 Hardware Interrupt Pin Masks
105-106 Vendor Specific
107 Reserved
108-110 Free Side Device Properties
111-112 Assigned for use by PCI Express
113 Free Side Device Properties
114-118 Reserved
119-122 Password Change Entry Area (Optional)
123-126 Password Entry Area (Optional)
127 Page Select Byte

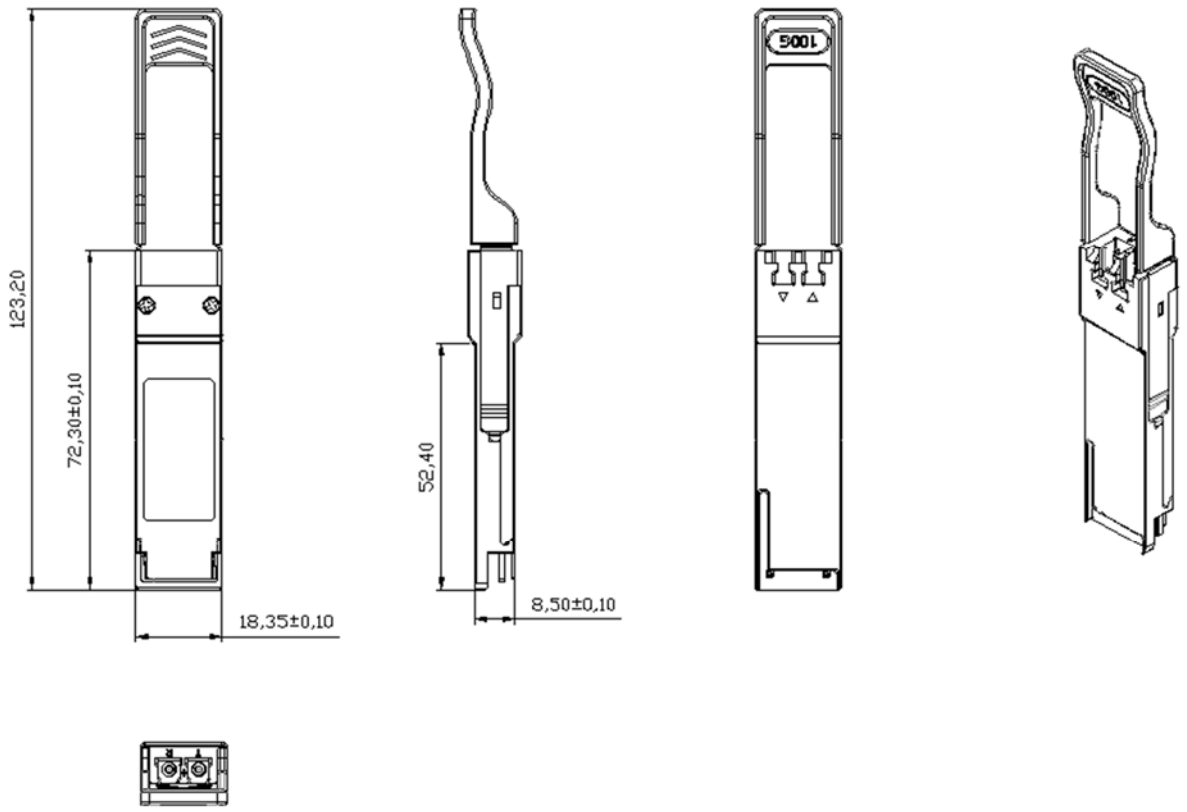
Upper Page 00h	Optional Page 01h	Optional Page 02h	Optional Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
	134-253 other entries		176-223 Channel Thresholds
192-223 Extended ID			224 Tx EQ & Rx Emphasis Magnitude ID
224-255 Vendor Specific ID			225 RX output amplitude indicators
			226-241 Channel Controls
			242-251 Channel Monitor Masks
	254-255 Application Code Entry TL		252-255 Reserved

Figure 2 – Two-Wire Interface Fields

The operating and diagnostic information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. The 2-wire serial interface consists of a master and a slave. The host side is the master, and the module side is the slave. Control and data are transferred serially. The master initiates all data transfers. Data can be transferred from the master to the slave and from the slave to the master.

The 2-wire interface consists of serial clock (SCL) and serial data (SDA) signals. The master uses SCL to clock data and control information on the 2-wire bus. The master and slave latch the state of SDA on the rising edge of SCL. The SDA signal is bidirectional. During data transfer, the SDA signal transitions when SCL is low. A transition on SDA while SCL is high indicates a Start or Stop condition. For more information, please refer to the QSFP28 MSA documentation.

Mechanical Specifications



Unit: mm

Ordering Information

Part Number	Product Description
CSMQ28HGL3140	100 Gbps QSFP28 ER4, LC, 40 km, 0 °C to +70 °C, with DDM

For More Information

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