CSMQDDQGM85M1

400 Gbps QSFP-DD SR4 Optical Transceiver

Description

The CSMQDDQGM85M1 is a 400 Gbps QSFP-DD SR4 optical transceiver designed for 100 m optical communication applications. The module converts eight channels of 50 Gbps PAM4 electrical input data into four channels of parallel optical signals, each operating at 100 Gbps, for an aggregate data rate of 400 Gbps. On the receiver side, the module converts four 100 Gbps parallel optical signals into eight channels of 50 Gbps PAM4 electrical output data. An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP-DD SR4 module receptacle. Host FEC is required to support up to 100 m fiber transmission.

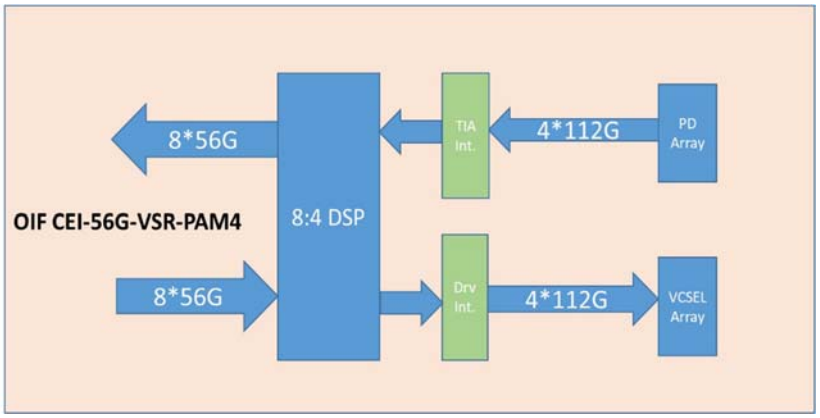
Features

- Compliant with QSFP-DD MSA
- Compliant with CMIS 4.0
- Parallel 4 Optical Lanes
- Compliant with IEEE 802.3db 400GBASE-SR4 Specification
- 8 × 53.125 Gbps Electrical Interface (400GAUI-8)
- Up to 100 m Transmission over OM4 MMF
- Maximum Power Consumption 9 W
- MPO-12 Receptacle
- Single +3.3 V Power Supply
- Case Temperature Range: 0 °C to +70 °C
- RoHS 2.0 Compliant

Applications

- 400G Ethernet
- Data Center Interconnect
- Enterprise Networking

Module Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature	TSTG	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	+3.6	V
Relative Humidity	RH	10	90%	Non-Condensing

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Case Temperature- Operating	TCASE	0	70	ºC
Supply Voltage	V_{CC}	3.135	3.465	V
Power Consumption	PDISS		9	W
Pre-FEC Bit Error Ratio			2.4×10^{-4}	
Link Distance over OM3		0.5	60	m
Link Distance over OM4		0.5	100	m

Electrical Specifications

Low-Speed Interface

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max) = 3.0 mA for Fast-mode, 20 mA for Fast-mode Plus
	VOH	VCC-0.5	VCC+0.3	V	
SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
Capacitance for SCL and SDA I/O PIN	Ci		14	pF	
Total Bus Capacitive Load for SCL and SDA	Cb		100	pF	3.0 kOhm Pull-Up Resistor, Max.
			200	pF	1.6 kOhm Pull-Up Resistor, Max.
LPMode/TxDis, ResetL, and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	10 kOhm Pull-Up to Host V_{CC}
ModPrsL	VOL				IOL=2.0mA
	VOH				ModPrsL can be implemented as a short circuit to GND on the module.

High-Speed Interface

Parameter	Min	Typical	Max	Unit	Notes
Receiver Electrical Output Characteristics at TP4					
Signaling Rate per Lane		26.5625		GBd	
AC Common-Mode Output Voltage (RMS)		-	17.5	mV	
Differential Peak-to-Peak Output Voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)		TBD		UI	
Near-End Eye Height, Differential	24			mV	
Near-End Vertical Eye Closure			7.5	dB	
Far-end ESMW (Eye symmetry mask width)		TBD		UI	
Far-End Eye Height, Differential	24			mV	
Far-End Vertical Eye Closure			7.5	dB	
Far-End Pre-Cursor ISI Ratio		TBD		%	
Common-Mode to Differential-Mode Conversion Return Loss	IEEE 802.3ck Equation (120G-1)			dB	
Effective return loss	TBD			dB	

Differential termination mismatch			10	%	
Transition time (min, 20% to 80%)		TBD		ps	
DC common mode voltage	-350		2850	mV	
Transmitter Electrical Input Characteristics at TP1					
Signaling rate, per lane		26.5625		GBd	
Differential pk-pk input voltage tolerance	900			mV	
Common-Mode to Differential-Mode Return Loss	IEEE 802.3ck Equation (120G-1)			dB	
Effective Return Loss	TBD				
Differential Termination Mismatch			10	%	
Module Stressed Input Test	See 120G.3.4.1				
Single-Ended Voltage Tolerance Range	-0.4		3.3	V	
DC Common-Mode Voltage	-350 2850			mV	

Optical Specifications

Transmitter				
Signaling Rate per Lane	53.125 ± 100 ppm			GBd
Lane Wavelength Range		850		nm
RMS Spectral Width			0.6	nm
Modulation Format	PAM4			
Average Optical Power per lane	-4.6		4	dBm
Amplitude (OMAouter), per Lane for TECQ ≤ 1.8 dB for 1.8 dB < TECQ ≤ 4.4 dB	-2.6 -4.4 + TECQ		3.5	dBm
Transmitter and Dispersion Eye Closure for PAM4, per Lane			4.4	dB
Transmitter Eye Closure for PAM4 (TECQ), per Lane			4.4	dB
Extinction Ratio	2.5			dB
Transmitter Excursion, per Lane			2	dB
Transmitter Transition Time, per Lane			17	ps
Average Launch Power per Lane at TX Off State			-30	dBm
Relative Intensity Noise (OMA)			-131	dB/Hz
Optical Return Loss Tolerance			12	dB

Receiver				
Signaling Rate per Lane	53.125 ± 100 ppm			GBd
Lane Wavelength Range		850		nm
Modulation Format	PAM4			
Damage Threshold	5			dBm
Average Receive Power, each lane	-6.4		4	dBm
Receiver Power, each lane (OMA)			3.5	dBm
Receiver Sensitivity per Lane (OMAouter) for TECQ ≤ 1.8 dB for 1.8 dB < TECQ ≤ 4.4 dB			-4.6 -6.4 + TECQ	dBm
Receiver Reflectance			-12	dB
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		4.4		dB
RX_LOS Assert Min./Max.	-15.0			dBm
RX_LOS De-Assert Min./Max.			-8.9	dBm
RX_LOS Hysteresis		1.5		dB

Digital Diagnostic Specifications

Parameter	Specification	Unit
Temperature Monitor Absolute Error	± 3	°C
Supply Voltage Monitor Absolute Error	± 5	%
I_bias Monitor Absolute Error	± 10	%
Received Power (Rx) Monitor Absolute Error	± 3.0	dB
Transmit Power (Tx) Monitor Absolute Error	± 3.0	dB

Pin Diagram

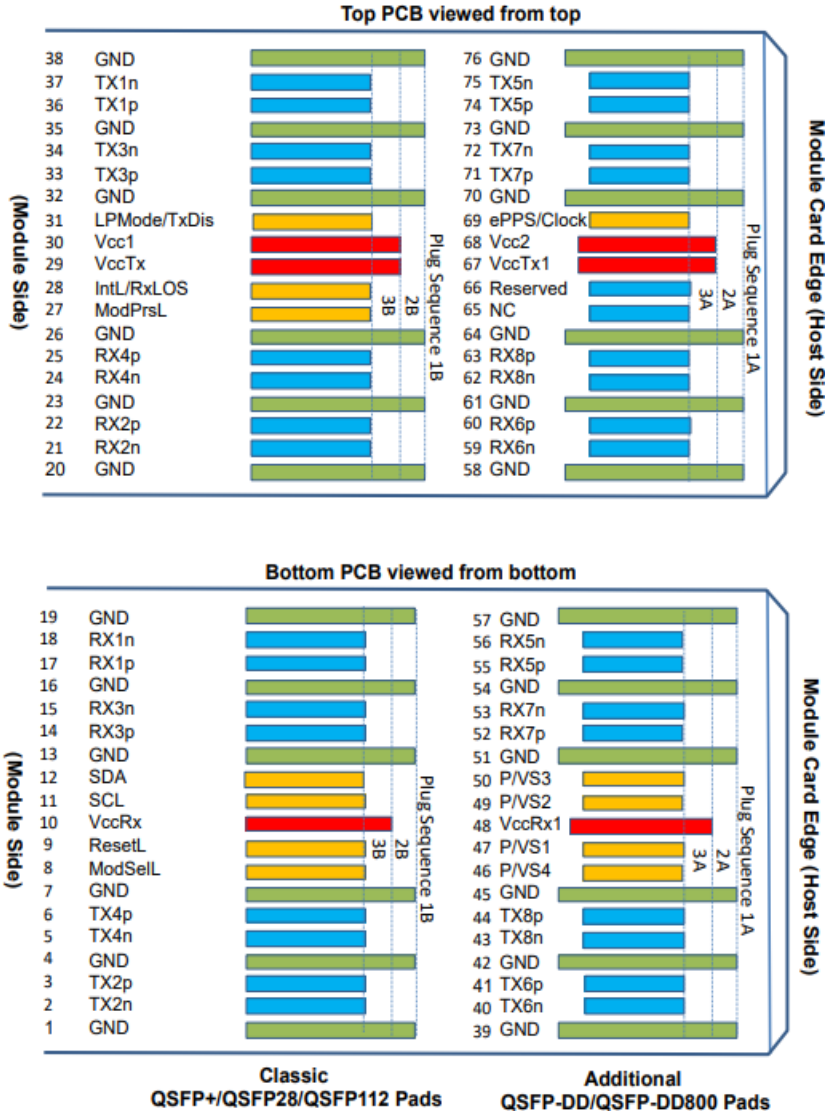


Figure 1 – QSFP-DD-Compliant 76-Pin Connector Pad Layout

Pin Definitions

Pin	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non - Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non - Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	

10		VccRx	+3.3 V Receiver Power Supply	2B	2
11	LVCMOS-I /O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non - Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non - Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non - Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non - Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL / RxLOS	Interrupt / Optional RxLOS	3B	
29		VccTx	+3.3 V Transmitter Power Supply	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode / Optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non - Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non - Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non - Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non - Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	+3.3 V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5

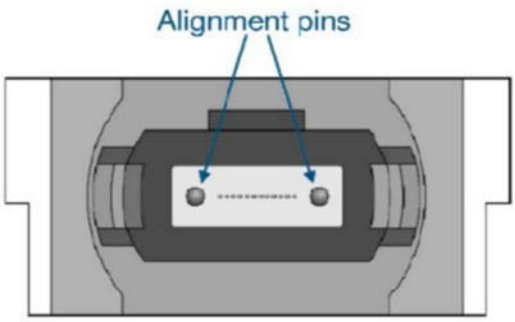
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non - Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non - Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non - Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non - Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	L VCMOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non - Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non - Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a steady-state current of 500 mA.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above, the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady-state current of 1500 mA.
3. Reserved and No Connect pads are recommended to be terminated with 10 kOhm to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure 2 for pad locations.) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, and then by 3A and 3B.
5. Full definitions of the P/VSx signals are currently under development. In new designs, unused P/VSx signals are recommended to be terminated on the host with 10 kOhm.

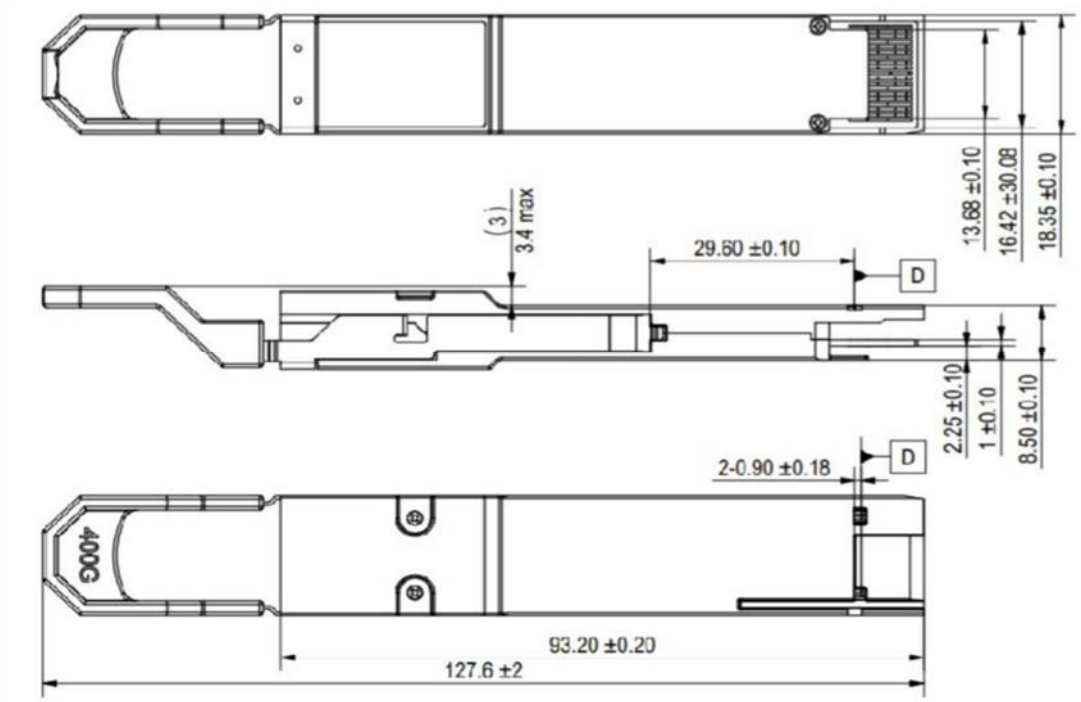
6. ePPS/Clock, if not used, is recommended to be terminated with 50 Ohm to ground on the host.

Optical Interface



Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

Mechanical Specifications



Unit: mm

Ordering Information

Part Number	Product Description
CSMQDDQGM85M1	400 Gbps, QSFP-DD SR4, 850 nm, 0 °C to +70 °C, MPO-12 APC

For More Information

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