KT330J
SMART GATE DRIVE PHOTOCOUPLER

Description

The KT330J is an advanced 1.5 A output current, easy to-use, intelligent gate driver which makes IGBT VCE fault protection compact, affordable, and easy-to implement. Features such as integrated VCE detection, under voltage lockout (UVLO), "soft" IGBT turn-off, isolated open collector fault feedback and active Miller clamping provide maximum design flexibility and circuit protection.

The KT330J contains a LED. The LED is optically coupled to an integrated circuit with a power output stage. It is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The voltage and current supplied by these photo couplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V and 100 A. For IGBTs with higher ratings, the KT330J can be used to drive a discrete power stage which drives the IGBT gate.

The KT330J has an insulation voltage of VIORM = 1414 VPEAK.

Features

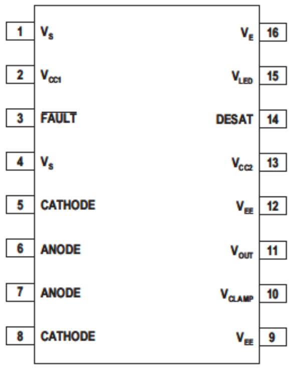
- 1.5 A maximum peak output current
- 1.0 A minimum peak output current
- 250 ns maximum propagation delay over temperature range
- 1.0A Active Miller Clamp. Clamp pin short to VEE if not in used
- Miller Clamping
- Desaturation Detection
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- "Soft" IGBT Turn-off
- Automatic Fault Reset after fixed Mute Time , typically 26us
- Available in SO-16 package
- 100 ns maximum pulse width distortion (PWD)
- 50 kV/μs minimum common mode rejection (CMR) at VCM = 1500 V
- ICC(max) < 5 mA maximum supply current
- Wide VCC operating range: 15 V to 30 V over temperature range
- Wide operating temperature range: –40°C to 110°C

Agency Approvals:

• UL Approved : UL1577

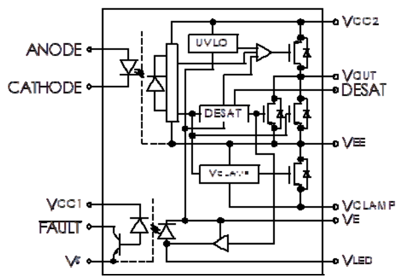
• VDE Approved : DIN EN60747-5-5

Schematic



1.VS	16.VE
2.VCC1	15.VLED
3.FAULT	14.DESAT
4.VS	13.VCC2
5.CATHODE	12.VEE
6.ANODE	11.VOUT
7.ANODE	10.VCLAMP
8.CATHODE	9.VEE

Internal Circuit



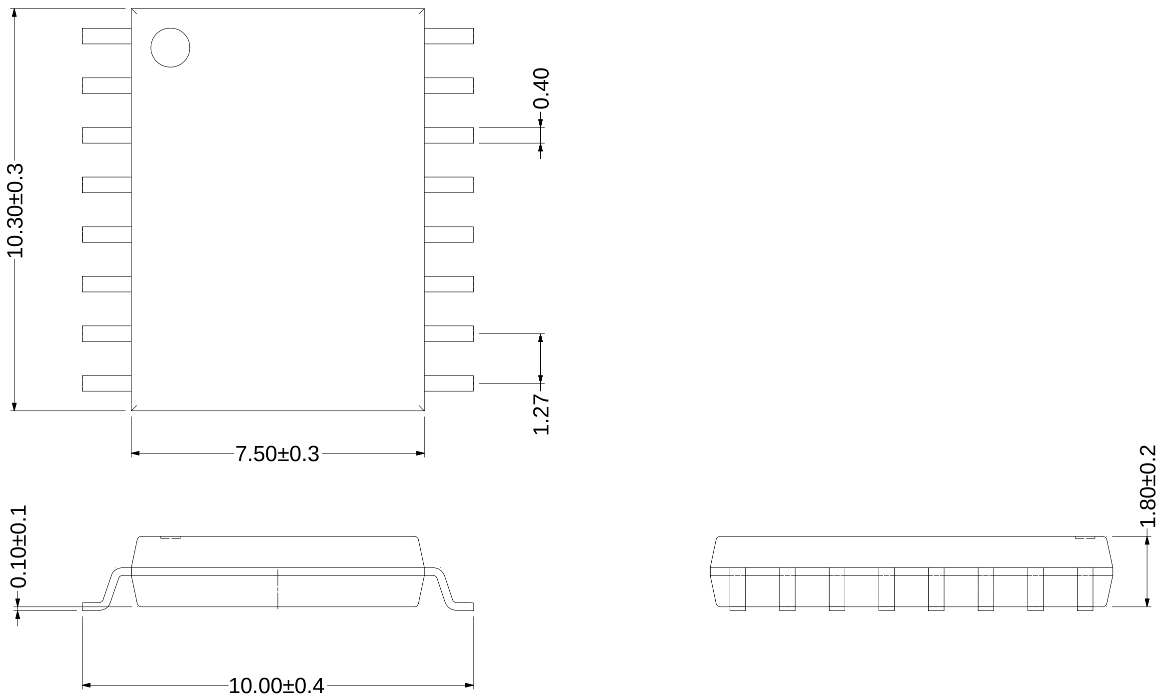
● Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters and Uninterruptible Power Supply(UPS)

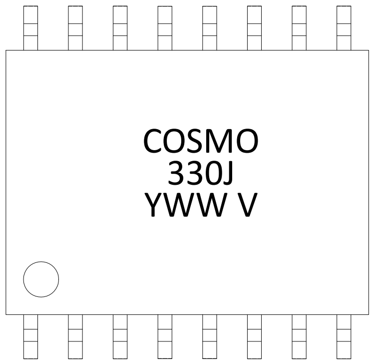
● Outside Dimension

Surface Mount Lead Forming

(Unit : mm)



● Device Marking



Notes:

cosmo
330J
YWW　　Y: Year code / WW: Week code
□　　V or None: VDE Option

Absolute Maximum Ratings

(Ta = 25°C)

Parameter		Symbol	Rating	Unit
Input	Forward current [1]	I_F	20	mA
	Peak transient forward current (<1 μs pulse width, 300pps)t	I_{FPT}	1	A
	Reverse voltage	V_R	5	V
Output	"H" peak output current [3]	$I_{OH(PEAK)}$	1.5	A
	"L" peak output current [3]	$I_{OL(PEAK)}$	1.5	A
	Output voltage	$V_{O(PEAK)}$	-0.5~V_{CC2}	V
	Positive Input Supply Voltage	V_{CC1}	-0.5~7.0	V
	FAULT Output Current	I_{FAULT}	8.0	mA
	FAULT Pin Voltage	V_{FAULT}	-0.5~V_{CC1}	V
	Negative Output Supply Voltage [6]	$(V_E - V_{EE})$	15	V
	Positive Output Supply Voltage	$(V_{CC2} - V_E)$	-0.5~35-(V_E-V_{EE})	V
	Peak Clamping Sinking Current	I_{Clamp}	1.0	A
	Total output supply voltage	V_{CC2}-V_{EE}	-0.5~35	V
	Miller Clamping Pin Voltage	V_{Clamp}	-0.5~Vcc2	V
	DESAT Voltage	V_{DESAT}	VE+10	V
	Junction temperature [2]	T_J	125	°C
Input IC Power Dissipation [2]		P_I	150	mW
Output IC Power Dissipation [2]		P_O	600	mW
Operating temperature range [2]		T_{opr}	-40~110	°C
Storage temperature range		T_{stg}	-55~125	°C
Lead soldering temperature(10s)		T_{sol}	260	°C
Isolation voltage (t=1min.,R.H ≤ 40%~60%) [24 25]		V_{ISO}	5000	V

Recommend Operation Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature [2]	T_A	-40	110	°C
Total Output Supply Voltage [7]	$(V_{CC2} - V_{EE})$	15	30	V
Negative Output Supply Voltage [4]	$(V_E - V_{EE})$	0	15	V
Positive Output Supply Voltage	$(V_{CC2} - V_E)$	15	30-(V_E-V_{EE})	V
Input Current (ON)	$I_{F(ON)}$	8	12	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V

● Electrical Characteristics

(Ta = 25°C)

Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input forward voltage		V_F	I_F=10mA	1.6	2.0	2.4	V
Input reverse voltage		BV_R	I_R=10μA	5	—	—	V
Input capacitance		C_{IN}	V_F=0V, f=1MHz	—	70	—	pF
FAULT Logic Low Output Voltage		V_{FAULTL}	I_{FAULT} = 1.1 mA, V_{CC1} = 5.5V		0.01	0.4	V
			I_{FAULT} = 1.1 mA, V_{CC1} = 3.3V		0.02	0.4	V
FAULT Logic High Output Current		I_{FAULTH}	V_{FAULT} = 5.5 V, V_{CC1} = 5.5V		0.01	0.5	μA
			V_{FAULT} = 3.3 V, V_{CC1} = 3.3V		0.006	0.3	μA
Output current [5,3]	"H" level	I_{OH}	$V_O = V_{CC2} - 4$		-1	-0.3	A
			$V_O = V_{CC2} - 15$			-1	
	"L" level	I_{OL}	$V_O = V_{EE} + 2.5$	0.3	1		
			$V_O = V_{EE} + 15$	1			
Low Level Output Current During Fault Condition [6]		I_{OLF}	$V_{OUT} - V_{EE}$ = 14 V	70	110	230	mA
Output voltage [7,8,9,23]	"H" level	V_{OH}	I_O = -650 μA	V_{CC}-0.5	V_{CC}-0.1		V
	"L" level	V_{OL}	I_O = 100 mA		0.13	0.5	
Clamp Pin Threshold Voltage		V_{tClamp}			2.2		V
Clamp Low Level Sinking Current		I_{CL}	$V_O = V_{EE} + 2.5$	0.21	0.8		A
Supply current [9]	"H" level	I_{CC2H}	I_O = 0 mA		2.16	5	mA
	"L" level	I_{CC2L}	I_O = 0 mA		2.29	5	
Blanking Capacitor [9,10] Charging Current		I_{CHG}	V_{DESAT} = 2 V	0.13	-0.23	-0.33	mA
Blanking Capacitor Discharge Current		I_{DSCHG}	V_{DESAT} = 7.0 V	10	31		mA
DESAT Threshold [9]		V_{DESAT}	$V_{CC2} - V_E > V_{UVLO-}$	6	6.7	7.5	V
Threshold input current	"Output L→H"	I_{FLH}	I_O = 0 mA, V_O > 5 V		0.33	6	mA
Threshold input voltage	"Output H→L"	V_{FHL}		0.8	1.75		V
Under Voltage Lockout Threshold [7,9,11,12]		V_{UVLO+}	V_O > 5 V	10.5	11.5	12.5	V
		V_{UVLO-}	V_O < 5 V	9.2	10.5	11.1	V
UVLO Hysteresis		$UVLO_{HYS}$		0.4	1		V
Supply voltage		V_{CC}		15	—	30	V

Resistance (input-output) [25]	R_{I-O}	V_{I-O}=500VDC	—	10^{12}	—	Ω

All Typical values at Ta = 25°C and $V_{CC2} – V_{EE}$ = 30 V, V_E - V_{EE} = 0 V; unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

● Switching Characteristics

(Ta = 25°C)

Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time [13 15]	"L→H"	t_{PLH}	Rg = 20 Ω, Cg = 5 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 10 mA, V_{CC2} = 30 V	50	104	250	ns
	"H→L"	t_{PHL}		50	77	250	
Pulse Width Distortion [14 17]		PWD		-100	-	100	
Propagation Delay Difference Between Any Two Parts [16 17]		PDD (t_{PHL} - t_{PLH})		-150	-	150	
Output rise time		t_r		-	50	-	
Output fall time		t_f		-	45	-	
DESAT Sense to 90% VO Delay [19]		$t_{DESAT(90\%)}$	C_{DESAT} = 100pF, R_F=2.1kΩ, Rg = 20 Ω, Cg = 5 nF, V_{CC2} = 30 V	-	0.1	0.3	µs
DESAT Sense to 10% VO Delay		$t_{DESAT(10\%)}$	C_{DESAT} = 100pF, R_F=2.1kΩ , Rg = 20 Ω, Cg = 5 nF, V_{CC2} = 30 V	-	1.1	1.5	µs
DESAT Sense to Low Level FAULT Signal Delay [18]		$t_{DESAT(FAULT)}$	C_{DESAT} = 100 pF, R_F = 2.1 kΩ, C_F = Open, Rg = 20 Ω, Cg = 5 nF, V_{CC2} = 30 V	-	0.2	0.5	µs
			C_{DESAT} = 100 pF, R_F = 2.1kΩ, C_F = 1 nF, Rg = 20 Ω, Cg = 5 nF, V_{CC2} = 30 V	-	0.8	-	µs
DESAT Sense to DESAT Low Propagation Delay [19]		$t_{DESAT(LOW)}$	C_{DESAT} = 100pF, R_F = 2.1kΩ, Rg = 20 Ω, Cg = 5 nF, V_{CC2} = 30 V	-	0.15	-	µs
DESAT Input Mute [20]		$t_{DESAT(MUTE)}$	C_{DESAT} = 100pF, R_F = 2.1kΩ, Rg = 20 Ω, Cg = 5 nF, V_{CC1} = 5.5V, V_{CC2} = 30 V	15	26	40	µs
Common mode transient immunity at high level output [21 26]		CM_H	T_A = 25°C, I_F = 10 mA V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1 kΩ, C_F = 15 pF	15			KV/µs
			T_A = 25°C, I_F = 10 mA V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1 kΩ, C_F = 1 nF	50			

Common mode transient immunity at low level output [22]	CM_L	T_A = 25°C, V_F = 0 V V_{CM} = 1500 V, V_{CC2} = 30 V, RF = 2.1 kΩ, C_F = 15 pF	15			KV/μs
		T_A = 25°C, V_F = 0 V V_{CM} = 1500 V, VCC2 = 30 V, R_F = 2.1 kΩ, C_F = 1 nF	50			

All Typical values at Ta = 25°C and $V_{CC2} - V_{EE}$ = 30 V, V_E - V_{EE} = 0 V; unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.
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Notes:
1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
2. In order to achieve the absolute maximum power dissipation specified, pins 4, 9, and 10 require ground plane connections and may require airflow. See the Thermal Model section in the application notes at the end of this data sheet for details on how to estimate junction temperature and power dissipation. In most cases the absolute maximum output IC junction temperature is the limiting factor. The actual power dissipation achievable will depend on the application environment (PCB Layout, air flow, part placement, etc.). See the Recommended PCB Layout section in the application notes for layout considerations. Output IC power dissipation is derated linearly at 10 mW/°C above 90°C. Input IC power dissipation does not require derating.
3. Maximum pulse width = 10 μs. This value is intended to allow for component tolerances for designs with I_O peak minimum = 1.0 A. Derate linearly from 2.0 A at +25°C to 1.5 A at +105°C. This compensates for increased I_{OPEAK} due to changes in V_{OL} over temperature.
4. This supply is optional. Required only when negative gate drive is implemented.
5. Maximum pulse width = 50 μs.
6. See the Slow IGBT Gate Discharge During Fault Condition section in the applications notes at the end of this data sheet for further details.
7. 15 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 12.5 V. For High Level Output Voltage testing, V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero units.
8. Maximum pulse width = 1.0 ms.
9. Once V_O of the KT330J is allowed to go high (V_{CC2} - V_E > V_{UVLO+}), the DESAT detection feature of the KT330J will be the primary source of IGBT protection. UVLO is needed to ensure D_{ESAT} is functional. Once V_{CC2} is increased from 0V to above V_{UVLO+}, DESAT will remain functional until V_{CC2} is decreased below V_{UVLO-}. Thus, the DESAT detection and UVLO features of the KT330J work in conjunction to ensure constant IGBT protection.
10. See the DESAT fault detection blanking time section in the applications notes at the end of this data sheet for further details.
11. This is the “increasing” (i.e. turn-on or “positive going” direction) of V_{CC2} - V_E
12. This is the “decreasing” (i.e. turn-off or “negative going” direction) of V_{CC2} - V_E
13. This load condition approximates the gate load of a 1200 V/75A IGBT.
14. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.
15. As measured from IF to V_O.
16. The difference between t_{PHL} and t_{PLH} between any two KT330J parts under the same test conditions.
17. As measured from ANODE, CATHODE of LED to V_{OUT}
18. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.
19. This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low. This is supply voltage dependent.
20. Auto Reset: This is the amount of time when V_{OUT} will be asserted low after DESAT threshold is exceeded. See the Description of Operation (Auto Reset) topic in the application information section.
21. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15 V or FAULT > 2 V).
22. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V or FAULT < 0.8 V).

23. To clamp the output voltage at V_{CC} - 3 $_{VBE}$, a pull-down resistor between the output and V_{EE} is recommended to sink a static current of 650 μA while the output is high. See the Output Pull-Down Resistor section in the application notes at the end of this data sheet if an output pull-down resistor is not used.
24. In accordance with UL 1577, each photo coupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
25. This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together. Split resistors network with a ratio of 1:1 is needed at input LED1.

TYPICAL PERFORMANCE CURVES & TEST CIRCUITS

Fig.1 VOH vs. temperature

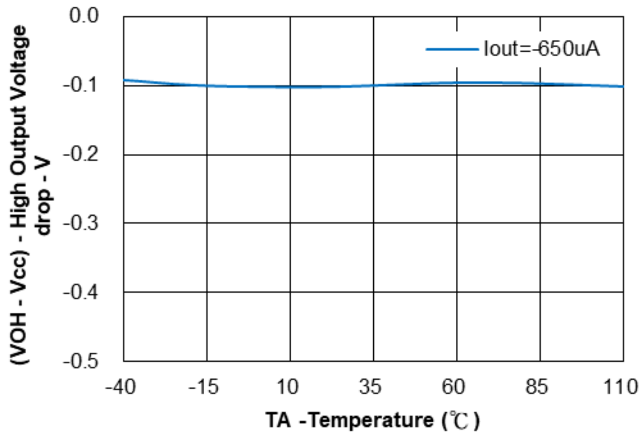


Fig.2 VOL vs. temperature

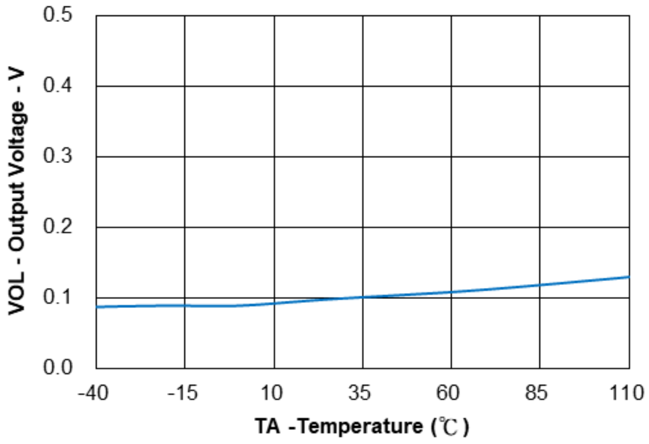


Fig.3 VOH vs. IOH

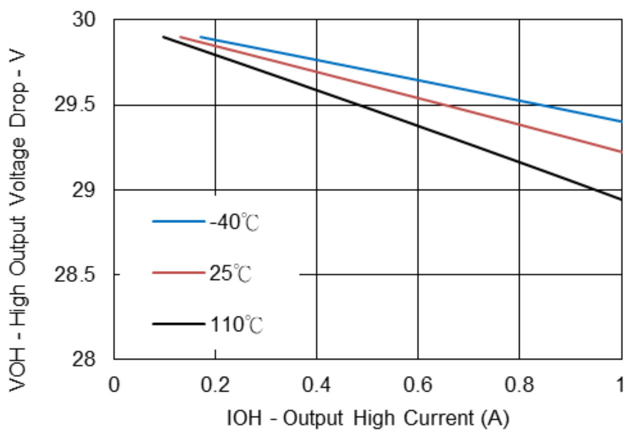


Fig.4 VOL vs. IOL

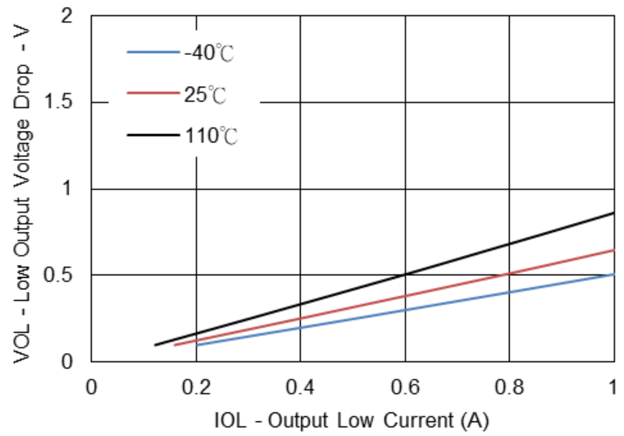


Fig.5 ICL vs. temperature

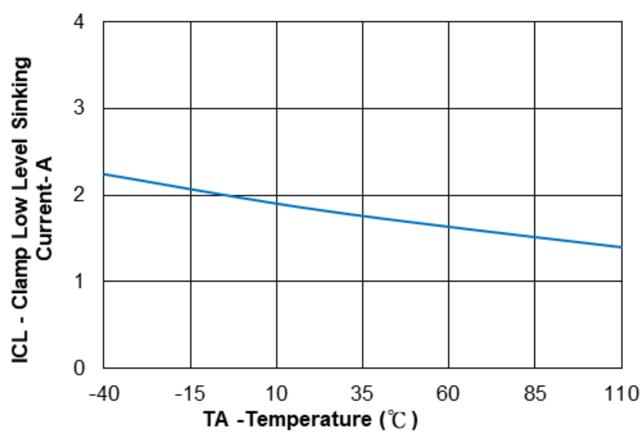


Fig.6 ICC2 vs. temperature

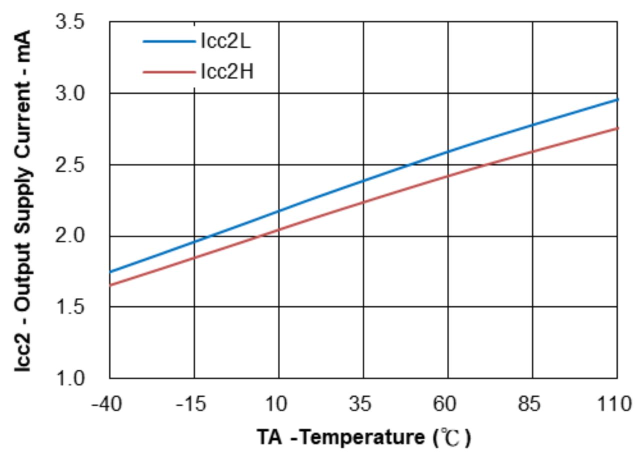


Fig.7 ICC2 vs. VCC2

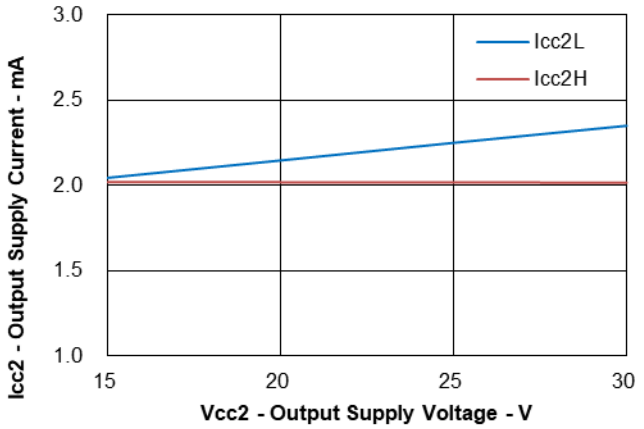


Fig.8 ICHG vs. temperature

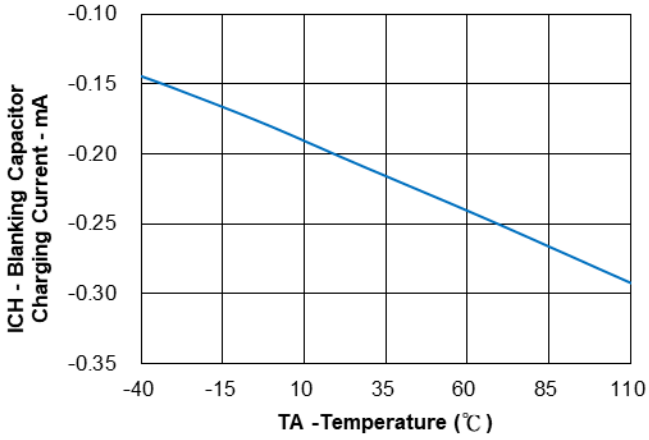


Fig.9 DESAT threshold vs. temperature

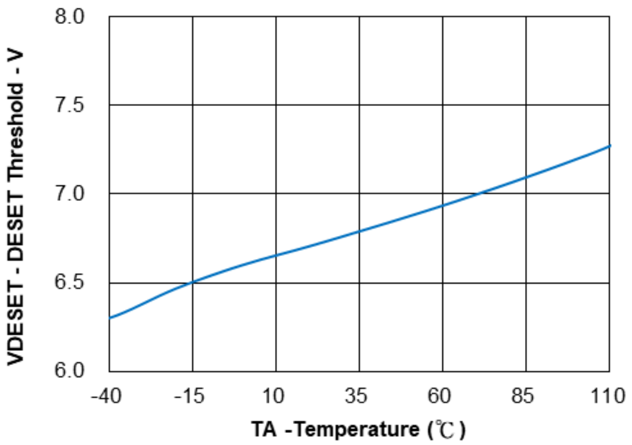


Fig.10 Propagation delay vs. temperature

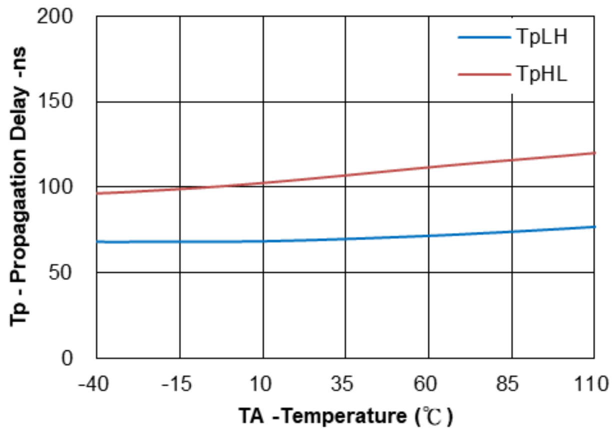


Fig.11 Propagation delay vs. supply voltage

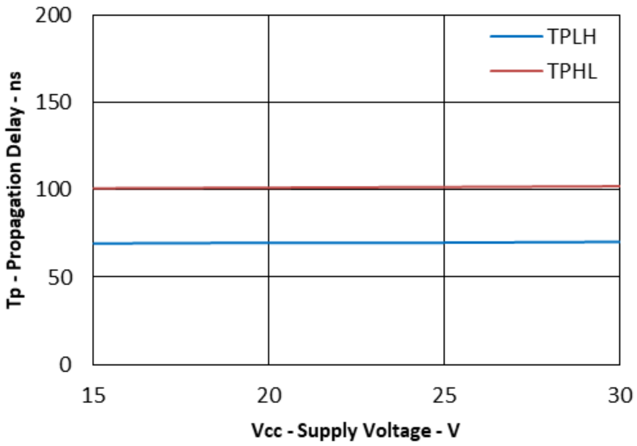


Fig.12 Propagation delay vs. RL

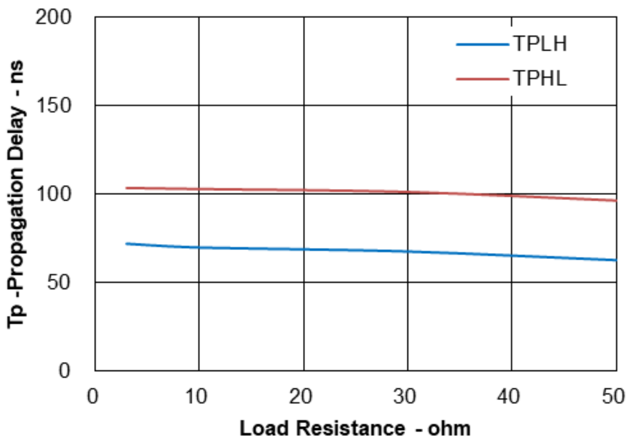


Fig.13 Propagation delay vs. CL

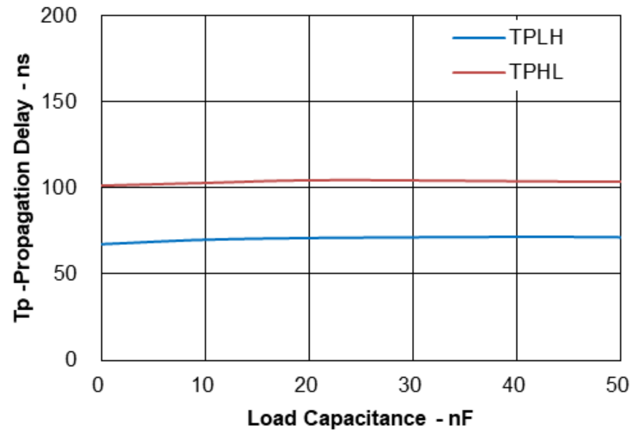


Fig.14 TDESAT90% vs. temperature

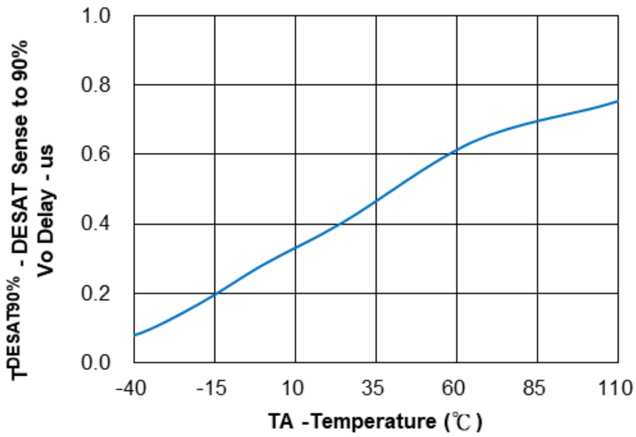


Fig.15 TDESAT10% vs. temperature

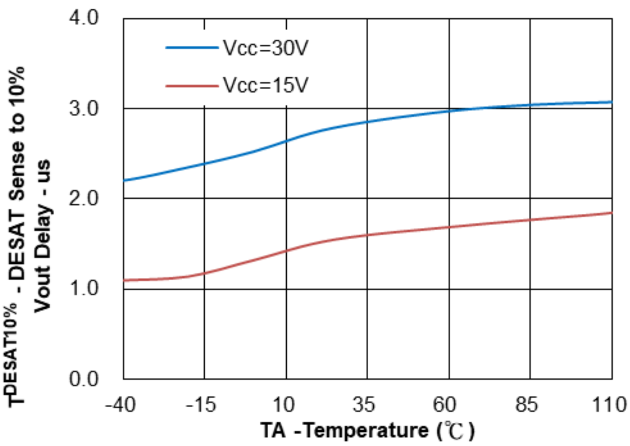


Fig.16 TDESAT10% vs. RL

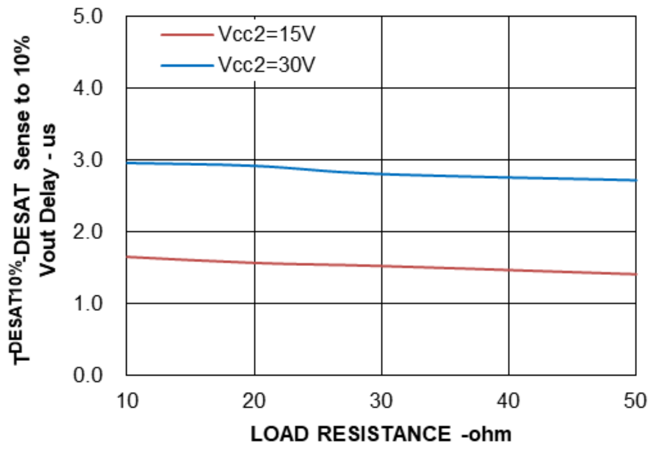


Fig.17 TDESAT10% vs. CL

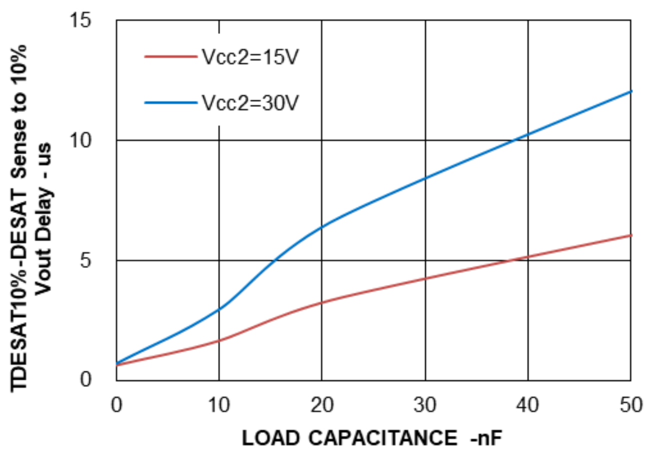


Fig.18 IOH Pulsed test circuit

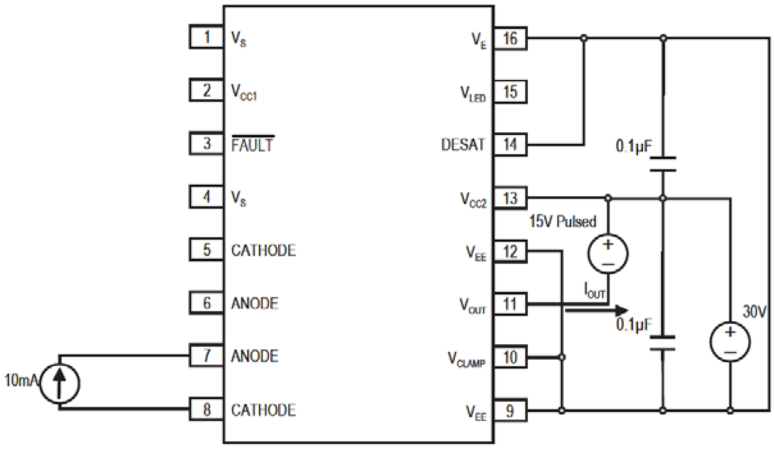


Fig.19 IOL Pulsed test circuit

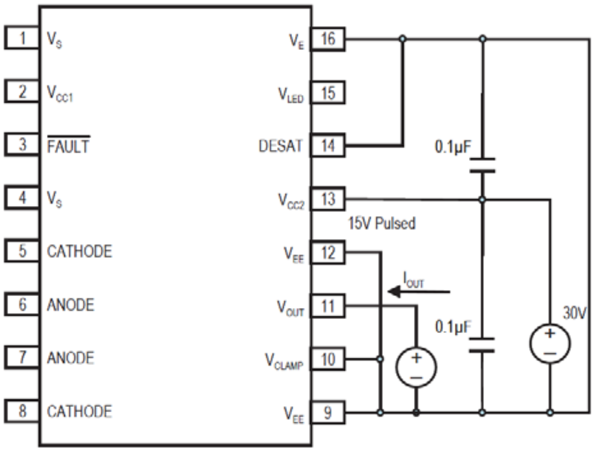


Fig.20 VOH Pulsed test circuit

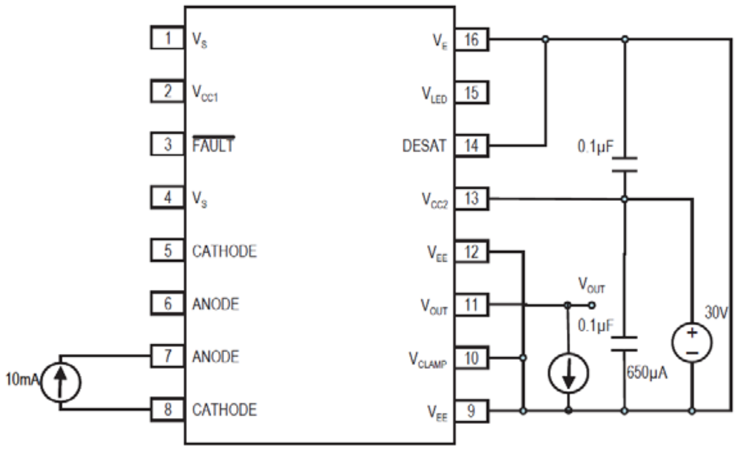


Fig.21 VOL Pulsed test circuit

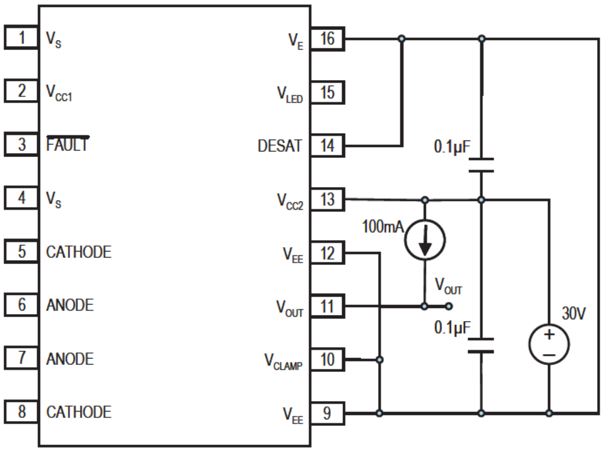


Fig.22 ICC2H test circuit

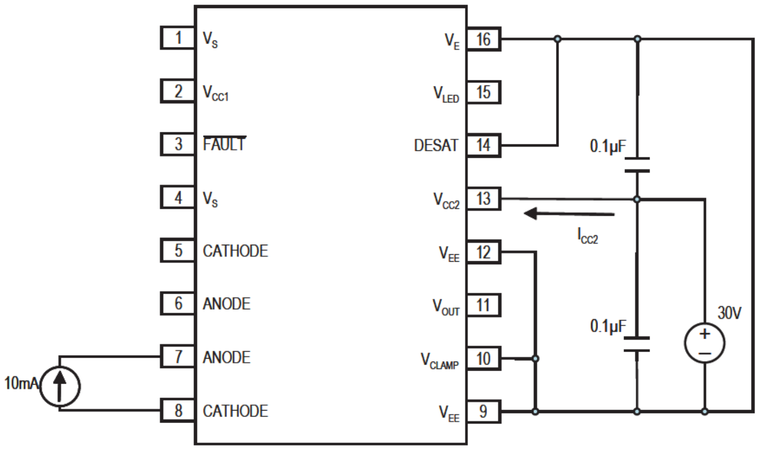


Fig.23 ICC2L test circuit

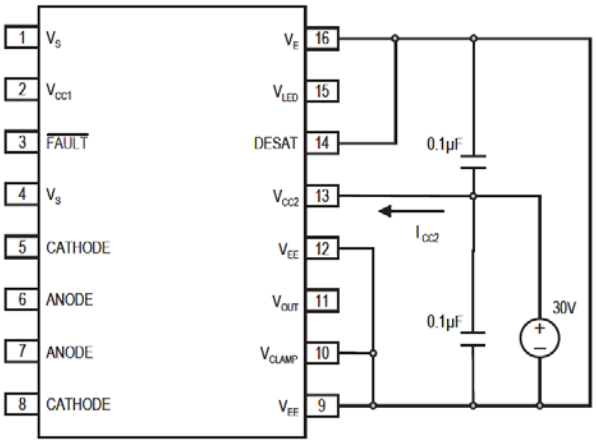


Fig.24 ICHG Pulsed test circuit

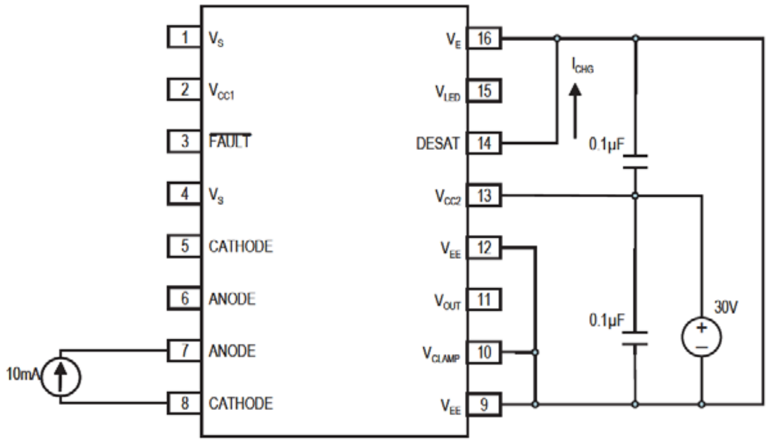


Fig.25 IDSCHG test circuit

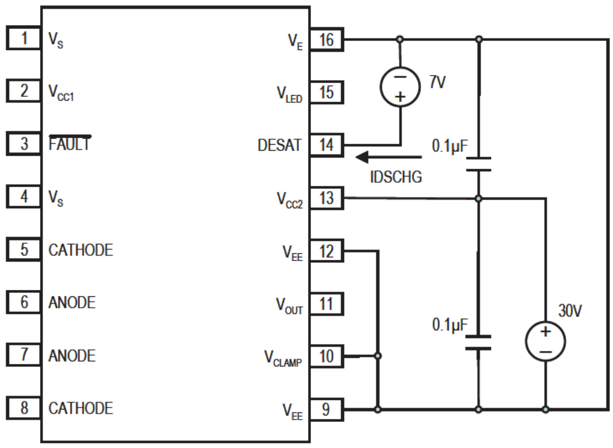


Fig.26 tPLH, tPHL, tf, tr, test circuit

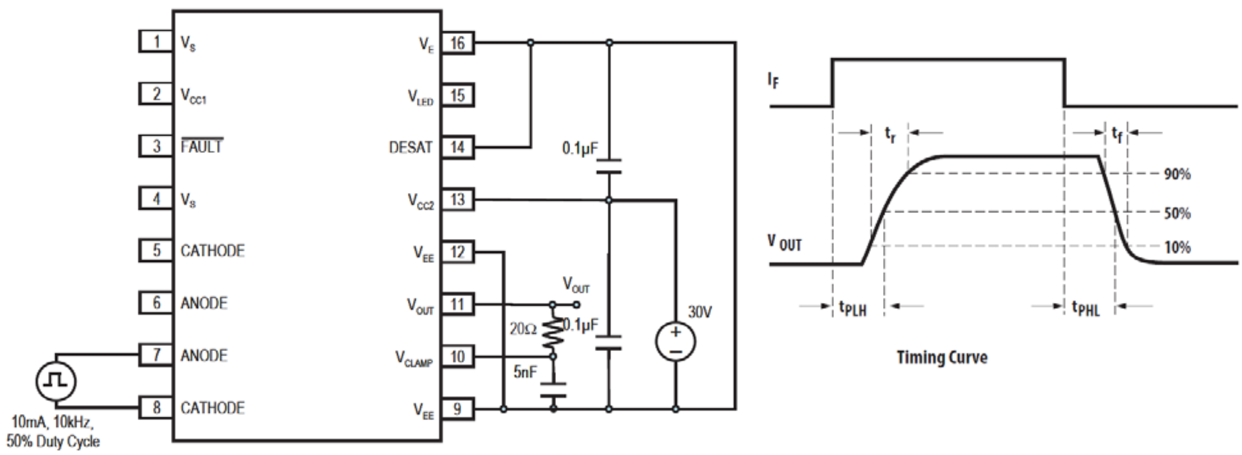
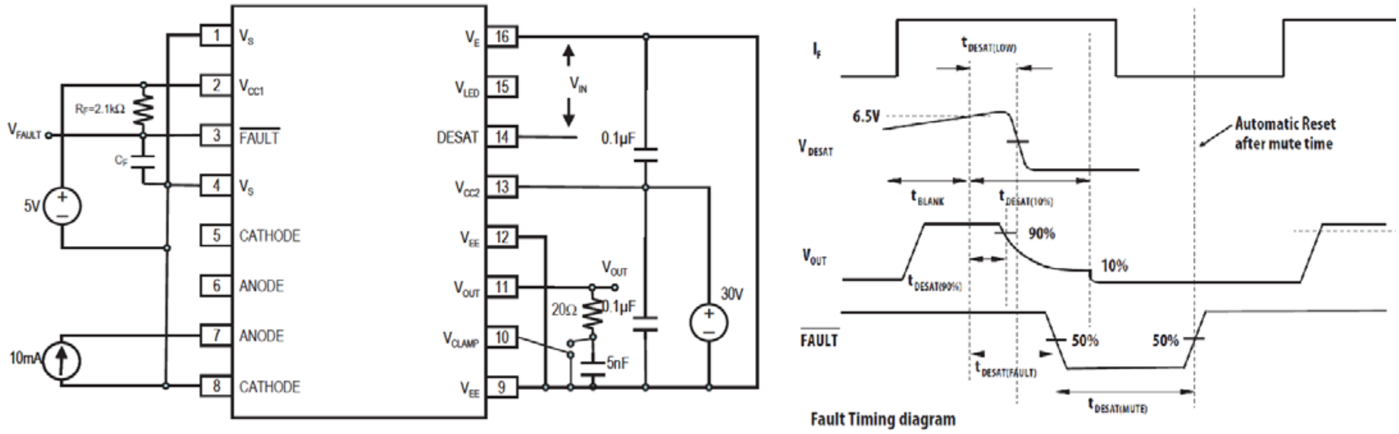


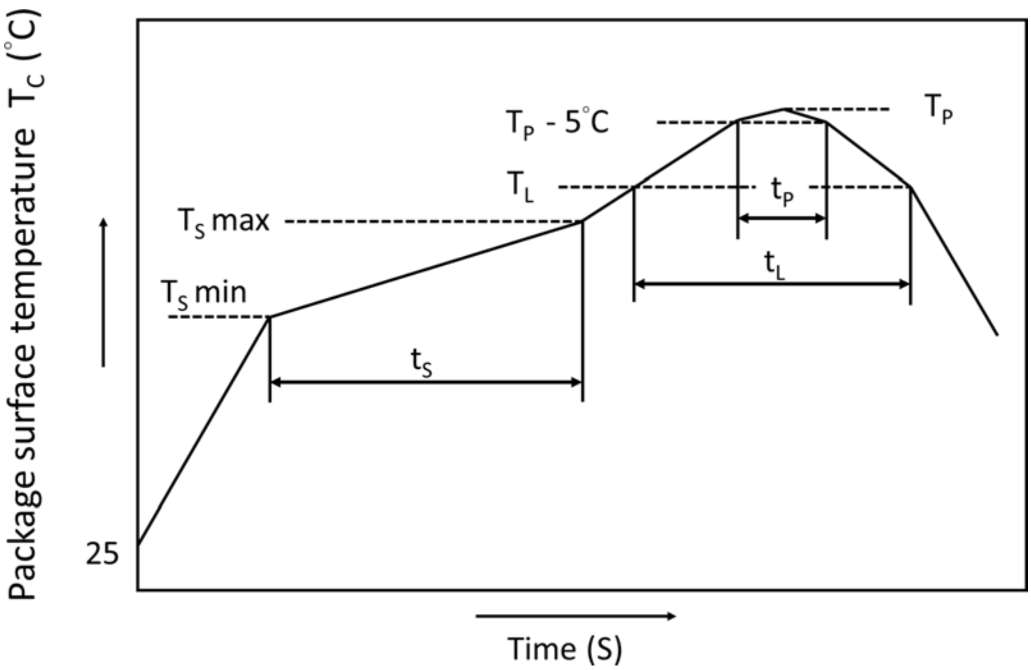
Fig.27 tDESAT fault test circuit



● Recommended Soldering Conditions

IR Reflow soldering：One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.

Recommended Temperature Profile of Infrared Reflow



Profile Item	Symbol	Min.	Max.	Unit
Preheat temperature	T_S	150	200	°C
Preheat time	t_S	60	120	s
Ramp-up rate (T_L to T_P)	-	—	3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	100	s
Peak Temperature	T_P	—	260	°C
Time during which T_C is between (T_P - 5) and T_P	t_P	—	20	s
Ramp-down rate	-	—	6	°C/s

Numbering System

KT330J (Y)-(Z)

Notes:

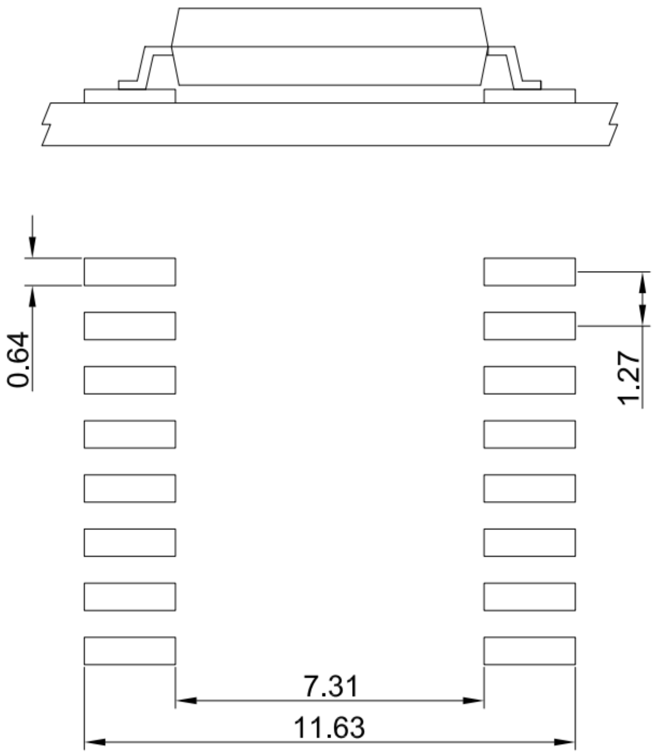
KT330J = Part No.

Y = Tape and reel option (TLD or TRU)

Z = VDE option (V or None)

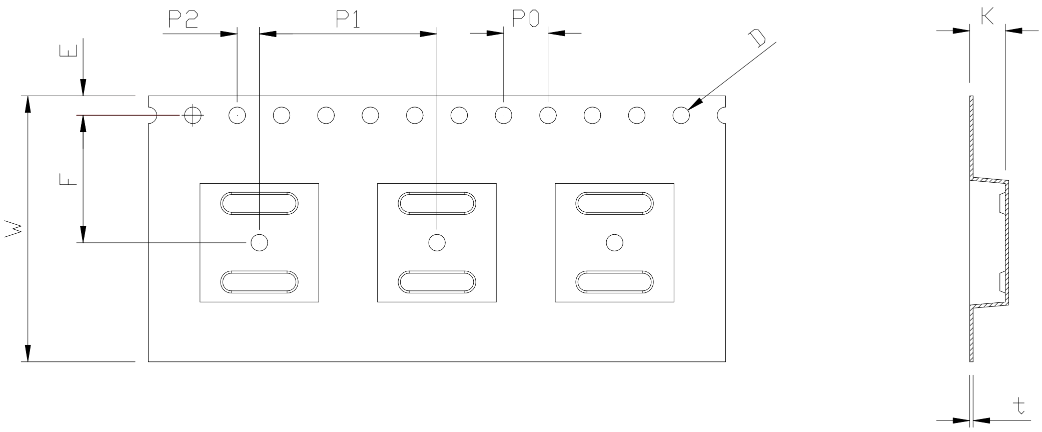
Option	Description	Packing quantity
(TLD)	surface mount type package + TLD tape & reel option	1000 units per reel
(TRU)	surface mount type package + TRU tape & reel option	1000 units per reel

Recommended Pad Layout for Surface Mount Lead Form



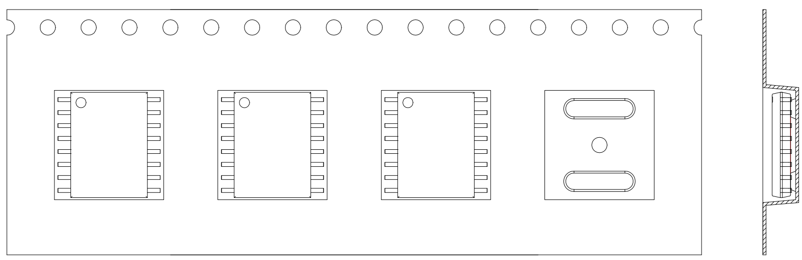
Unit :mm

● LSOP6 Carrier Tape & Reel

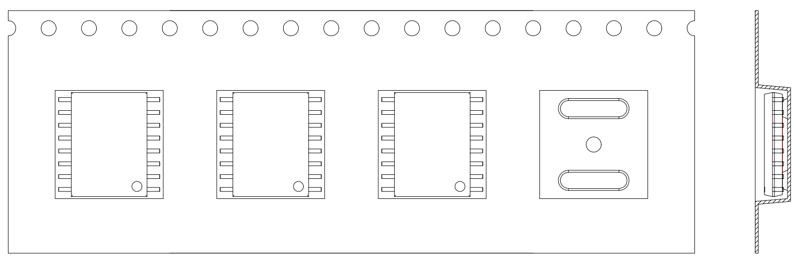


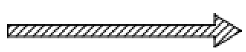
Dimension Symbol	D	E	F	P0	P1	P2	t	W	K
Dimension (mm)	1.5±0.1	1.75±0.1	11.5±0.1	4.0±0.1	16.0±0.1	2.0±0.1	0.3±0.1	24.0±0.3	3.2±0.1

TRU



TLD





Direction of feed from reel

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