

● Description

The KT5214 is an advanced 4 A output current, easy-to-use, intelligent gate driver which makes IGBT VCE fault protection compact, affordable, and easy-to-implement. Features such as integrated VCE detection, under voltage lockout (UVLO), “soft” IGBT turn-off, isolated open collector fault feedback and active Miller clamping provide maximum design flexibility and circuit protection.

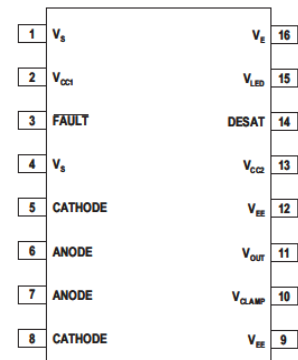
The KT5214 contains a LED. The LED is optically coupled to an integrated circuit with a power output stage. KT5214 is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V and 100 A. For IGBTs with higher ratings, the KT5214 can be used to drive a discrete power stage which drives the IGBT gate.

The KT5214 has an insulation voltage of $V_{IORM} = 1414 V_{PEAK}$.

● Features

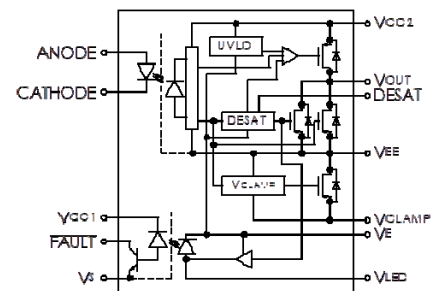
- 4.0 A maximum peak output current
- 250 ns maximum propagation delay over temperature range
- 1.7A Active Miller Clamp. Clamp pin short to V_{EE} if not in used
- Miller Clamping
- Desaturation Detection
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- “Soft” IGBT Turn-off
- Fault Reset by next LED turn-on (low to high) after fault mute period
- Available in SO-16 package
- 100 ns maximum pulse width distortion (PWD)
- 50 kV/ μ s minimum common mode rejection (CMR) at $V_{CM} = 1500 V$
- $I_{CC(max)} < 5 mA$ maximum supply current
- Wide V_{CC} operating range: 15 V to 30 V over temperature range
- Wide operating temperature range: $-40^{\circ}C$ to $110^{\circ}C$

● Schematic



1.VS	16.VE
2.VCC1	15.VLED
3.FAULT	14.DESAT
4.VS	13.VCC2
5.CATHODE	12.VEE
6.ANODE	11.VOUT
7.ANODE	10.VCLAMP
8.CATHODE	9.VEE

● Internal Circuit



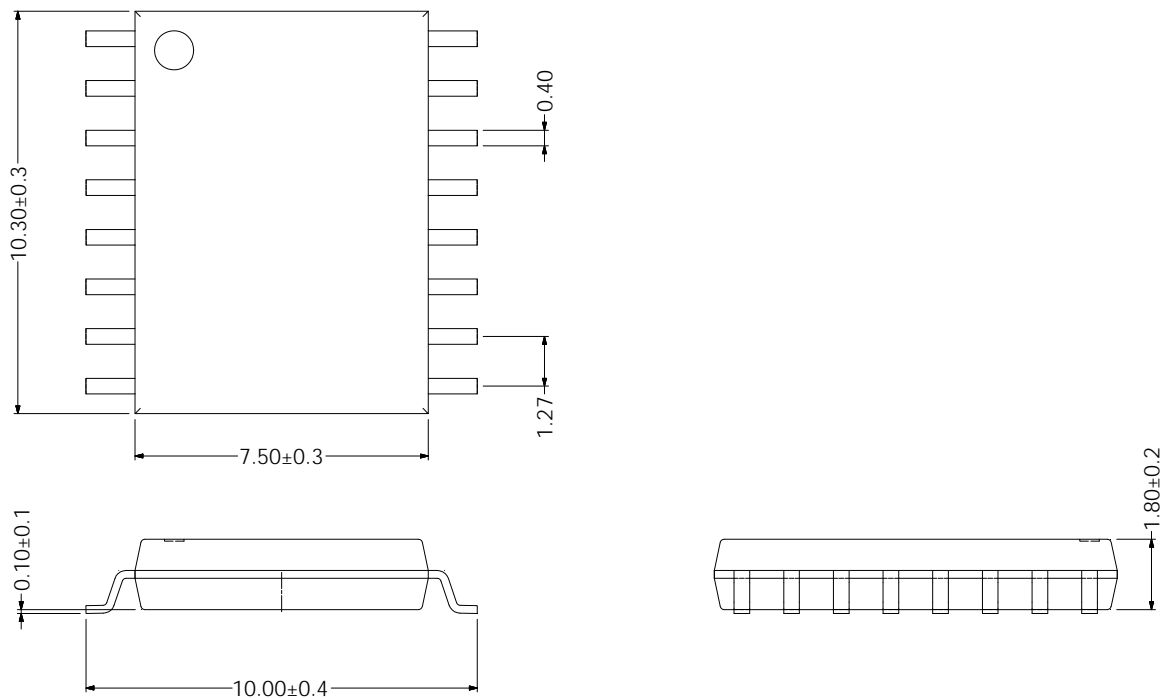
● **Applications**

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters and Uninterruptible Power Supply(UPS)

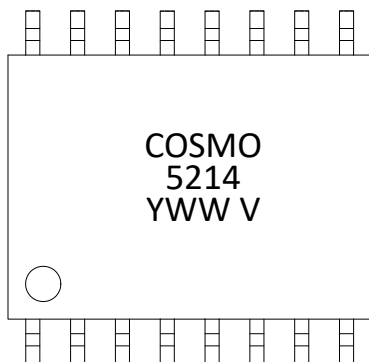
● **Outside Dimension**

Surface Mount Lead Forming

(Unit : mm)



● **Device Marking**



Notes:

COSMO
5214
YWW



Y: Year code / WW: Week code
V or None: VDE Option

● Absolute Maximum Ratings

(Ta = 25°C)

Parameter		Symbol	Rating	Unit
Input	Forward current ¹	I _F	20	mA
	Peak transient forward current (<1 μs pulse width, 300pps)t	I _{FPT}	1	A
	Reverse voltage	V _R	5	V
Output	"H" peak output current ³	I _{OH(PEAK)}	4	A
	"L" peak output current ³	I _{OL(PEAK)}	4	A
	Output voltage	V _{O(PEAK)}	-0.5~V _{CC2}	V
	Positive Input Supply Voltage	V _{CC1}	-0.5~7.0	V
	FAULT Output Current	I _{FAULT}	8.0	mA
	FAULT Pin Voltage	V _{FAULT}	-0.5~V _{CC1}	V
	Negative Output Supply Voltage ⁶	(V _E - V _{EE})	-0.5~15	V
	Positive Output Supply Voltage	(V _{CC2} - V _E)	-0.5~33-(V _E -V _{EE})	V
	Peak Clamping Sinking Current	I _{clamp}	1.7	A
	Total output supply voltage	V _{CC2} -V _{EE}	-0.5~33	V
	Miller Clamping Pin Voltage	V _{clamp}	-0.5~V _{CC2}	V
	DESAT Voltage	V _{DESAT}	VE~VE+10	V
	Junction temperature ²	T _J	125	°C
Input IC Power Dissipation ²		P _I	150	mW
Output IC Power Dissipation ²		P _O	600	mW
Operating temperature range ²		T _{opr}	-40~110	°C
Storage temperature range		T _{stg}	-55~125	°C
Lead soldering temperature(10s)		T _{sol}	260	°C
Isolation voltage (t=1min.,R.H ≤ 40%~60%) ^{24 25}		V _{ISO}	5000	V

● Recommend Operation Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature ²	T _A	-40	110	°C
Total Output Supply Voltage ⁷	(V _{CC2} - V _{EE})	15	30	V
Negative Output Supply Voltage ⁴	(V _E - V _{EE})	0	15	V
Positive Output Supply Voltage	(V _{CC2} - V _E)	15	30-(V _E -V _{EE})	V
Input Current (ON)	I _{F(ON)}	8	12	mA
Input Voltage (OFF)	V _{F(OFF)}	-3.6	0.8	V

● Electrical Characteristics

(Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Input forward voltage	V_F	$I_F = 10\text{mA}$	1.6	2.0	2.4	V	
Input reverse voltage	BV_R	$I_R = 10\mu\text{A}$	5	—	—	V	
Input capacitance	C_{IN}	$V_F = 0\text{V}, f = 1\text{MHz}$	—	70	—	pF	
FAULT Logic Low Output Voltage	V_{FAULTL}	$I_{FAULT} = 1.1\text{ mA}, V_{CC1} = 5.5\text{V}$	—	0.01	0.4	V	
		$I_{FAULT} = 1.1\text{ mA}, V_{CC1} = 3.3\text{V}$	—	0.02	0.4	V	
FAULT Logic High Output Current	I_{FAULTH}	$V_{FAULT} = 5.5\text{ V}, V_{CC1} = 5.5\text{V}$	—	0.01	0.5	μA	
		$V_{FAULT} = 3.3\text{ V}, V_{CC1} = 3.3\text{V}$	—	0.006	0.3	μA	
Output current ^{5 3}	"H" level	I_{OH}	$V_O = V_{CC2} - 4$	—	-2.9	-1.2	A
		$V_O = V_{CC2} - 15$	—	—	-4.0		
	"L" level	I_{OL}	$V_O = V_{EE} + 2.5$	1.2	3.1	—	
		$V_O = V_{EE} + 15$	4.0	—	—		
Low Level Output Current During Fault Condition ⁶	I_{OLF}	$V_{OUT} - V_{EE} = 14\text{ V}$	70	100	230	mA	
Output voltage ^{7 8 9 23}	"H" level	V_{OH}	$I_O = -100\text{mA}$	$V_{CC} - 0.5$	$V_{CC} - 0.1$	—	V
	"L" level	V_{OL}	$I_O = 100\text{ mA}$	—	0.1	0.5	
Clamp Pin Threshold Voltage	V_{Iclamp}	—	—	2.2	—	V	
Clamp Low Level Sinking Current	I_{CL}	$V_O = V_{EE} + 2.5$	0.5	1.5	—	A	
Supply current ⁹	"H" level	I_{CC2H}	$I_O = 0\text{ mA}$	—	2.23	5	mA
	"L" level	I_{CC2L}	$I_O = 0\text{ mA}$	—	2.36	5	
Blanking Capacitor ^{9 10} Charging Current	I_{CHG}	$V_{DESAT} = 2\text{ V}$	-0.13	-0.24	-0.33	mA	
Blanking Capacitor Discharge Current	I_{DSCHG}	$V_{DESAT} = 7.0\text{ V}$	10	31	—	mA	
DESAT Threshold ⁹	V_{DESAT}	$V_{CC2} - V_E > V_{UVLO-}$	6	6.7	7.5	V	
Threshold input current	"Output L→H"	I_{FLH}	$I_O = 0\text{ mA}, V_O > 5\text{ V}$	—	0.27	5	mA
Threshold input voltage	"Output H→L"	V_{FHL}	$I_O = 0\text{ mA}, V_O < 5\text{ V}$	0.8	1.74	—	V
Under Voltage Lockout Threshold ^{7 9 11 12}	V_{UVLO+}	$V_O > 5\text{ V}$	10.5	11.5	12.5	V	
	V_{UVLO-}	$V_O < 5\text{ V}$	9.2	10.5	11.1	V	
UVLO Hysteresis	$UVLO_{HYS}$	—	0.4	1	—	V	
Supply voltage	V_{CC}	—	15	—	30	V	
Resistance (input-output) ²⁵	R_{I-O}	$V_{I-O} = 500\text{VDC}$	—	10^{12}	—	Ω	

All Typical values at Ta = 25°C and $V_{CC2} - V_{EE} = 30\text{ V}$, $V_E - V_{EE} = 0\text{ V}$; unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

● Switching Characteristics

(Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time ^{13 15}	"L→H"	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%, If = 10 mA, VCC2 = 30 V	50	97	250	ns
	"H→L"		50	94	250	
Pulse Width Distortion ^{14 17}	PWD		-100	-	100	
Propagation Delay Difference Between Any Two Parts ^{16 17}	PDD (tPHL - tPLH)		-150	-	150	
Output rise time	tr		-	22	-	
Output fall time	tf		-	14	-	
DESAT Sense to 90% VO Delay ¹⁹	tDESAT(90%)	CDESAT = 100pF, RF=2.1kΩ, Rg = 10 Ω, Cg = 10 nF, VCC2 = 30 V	-	0.1	0.5	μs
DESAT Sense to 10% VO Delay	tDESAT(10%)	CDESAT = 100pF, RF=2.1kΩ , Rg = 10 Ω, Cg = 10 nF, VCC2 = 30 V	-	2.3	5	μs
DESAT Sense to Low Level FAULT Signal Delay ¹⁸	tDESAT(FAULT)	CDESAT = 100 pF, RF = 2.1 kΩ, CF = Open, Rg = 10 Ω, Cg = 10 nF, VCC2 = 30 V	-	0.2	0.5	μs
		CDESAT = 100 pF, RF = 2.1kΩ, CF = 1 nF, Rg = 10 Ω, Cg = 10 nF, VCC2 = 30 V	-	0.8	-	μs
DESAT Sense to DESAT Low Propagation Delay ¹⁹	tDESAT(LOW)	CDESAT = 100pF, RF = 2.1kΩ, Rg = 10 Ω, Cg = 10 nF, VCC2 = 30 V	-	0.15	-	μs
DESAT Input Mute ²⁰	tDESAT(MUTE)	CDESAT = 100pF, RF = 2.1kΩ, Rg = 10 Ω, Cg = 10 nF, VCC1 = 5.5V, VCC2 = 30 V	5	-	-	μs
RESET to High Level FAULT Signal Delay	tRESET(FAULT)	CDESAT = 100pF, RF = 2.1 kΩ,Rg = 10 Ω, Cg = 10 nF,VCC1 = 5.5V, VCC2 = 30 V	0.2	0.6	2.0	μs
		CDESAT = 100pF, RF = 2.1 kΩ,Rg = 10 Ω, Cg = 10 nF,VCC1 = 3.3V, VCC2 = 30 V	0.2	0.6	2.5	μs
Common mode transient immunity at high level output ²¹ ₂₆	CMH	TA = 25°C, IF = 10 mA VCM = 1500 V, VCC2 = 30 V, RF = 2.1 kΩ, CF = 15 pF	15	-	-	KV/μs

		$T_A = 25^\circ\text{C}$, $I_F = 10\text{ mA}$ $V_{CM} = 1500\text{ V}$, $V_{CC2} = 30\text{ V}$, $R_F = 2.1\text{ k}\Omega$, $C_F = 1\text{ nF}$	50	-	-	
Common mode transient immunity at low level output 22	CML	$T_A = 25^\circ\text{C}$, $V_F = 0\text{ V}$ $V_{CM} = 1500\text{ V}$, $V_{CC2} = 30\text{ V}$, $R_F = 2.1\text{ k}\Omega$, $C_F = 15\text{ pF}$	15	-	-	KV/ μs
		$T_A = 25^\circ\text{C}$, $V_F = 0\text{ V}$ $V_{CM} = 1500\text{ V}$, $V_{CC2} = 30\text{ V}$, $R_F = 2.1\text{ k}\Omega$, $C_F = 1\text{ nF}$	50	-	-	

All Typical values at $T_A = 25^\circ\text{C}$ and $V_{CC2} - V_{EE} = 30\text{ V}$, $V_E - V_{EE} = 0\text{ V}$; unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

Notes:

- Derate linearly above 70°C free air temperature at a rate of $0.3\text{ mA}/^\circ\text{C}$.
- In order to achieve the absolute maximum power dissipation specified, pins 4, 9, and 10 require ground plane connections and may require airflow. See the Thermal Model section in the application notes at the end of this data sheet for details on how to estimate junction temperature and power dissipation. In most cases the absolute maximum output IC junction temperature is the limiting factor. The actual power dissipation achievable will depend on the application environment (PCB Layout, air flow, part placement, etc.). See the Recommended PCB Layout section in the application notes for layout considerations. Output IC power dissipation is derated linearly at $10\text{ mW}/^\circ\text{C}$ above 90°C . Input IC power dissipation does not require derating.
- Exponential waveform pulse width $PW \leq 0.2\ \mu\text{s}$, $f \leq 15\text{ kHz}$, $V_{CC} = 15\text{ V}$.
- This supply is optional. Required only when negative gate drive is implemented.
- Maximum pulse width = $50\ \mu\text{s}$.
- See the Slow IGBT Gate Discharge During Fault Condition section in the applications notes at the end of this data sheet for further details.
- 15 V is the recommended minimum operating positive supply voltage ($V_{CC2} - V_E$) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 12.5 V . For High Level Output Voltage testing, V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero units.
- Maximum pulse width = 1.0 ms .
- Once V_O of the KT5214 is allowed to go high ($V_{CC2} - V_E > V_{UVLO+}$), the DESAT detection feature of the KT5214 will be the primary source of IGBT protection. UVLO is needed to ensure D_{ESAT} is functional. Once V_{CC2} is increased from 0 V to above V_{UVLO+} , DESAT will remain functional until V_{CC2} is decreased below V_{UVLO-} . Thus, the DESAT detection and UVLO features of the KT5214 work in conjunction to ensure constant IGBT protection.
- See the DESAT fault detection blanking time section in the applications notes at the end of this data sheet for further details.
- This is the "increasing" (i.e. turn-on or "positive going" direction) of $V_{CC2} - V_E$
- This is the "decreasing" (i.e. turn-off or "negative going" direction) of $V_{CC2} - V_E$
- This load condition approximates the gate load of a $1200\text{ V}/75\text{ A}$ IGBT.
- Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.
- As measured from I_F to V_O .

16. The difference between t_{PHL} and t_{PLH} between any two APCS-5214 parts under the same test conditions.
17. As measured from ANODE, CATHODE of LED to V_{OUT}
18. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.
19. This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low. This is supply voltage dependent.
20. Auto Reset: This is the amount of time when V_{OUT} will be asserted low after DESAT threshold is exceeded. See the Description of Operation (Auto Reset) topic in the application information section.
21. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM} , to assure that the output will remain in the high state (i.e., $V_O > 15\text{ V}$ or $FAULT > 2\text{ V}$).
22. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM} , to assure that the output will remain in a low state (i.e., $V_O < 1.0\text{ V}$ or $FAULT < 0.8\text{ V}$).
23. To clamp the output voltage at $V_{CC} - 3V_{BE}$, a pull-down resistor between the output and V_{EE} is recommended to sink a static current of $650\text{ }\mu\text{A}$ while the output is high. See the Output Pull-Down Resistor section in the application notes at the end of this data sheet if an output pull-down resistor is not used.
24. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 6000\text{ V}_{rms}$ for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
25. This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together.
26. Split resistors network with a ratio of 1:1 is needed at input LED1.

• TYPICAL PERFORMANCE CURVES & TEST CIRCUITS

Fig.1 IOH vs. Temperature

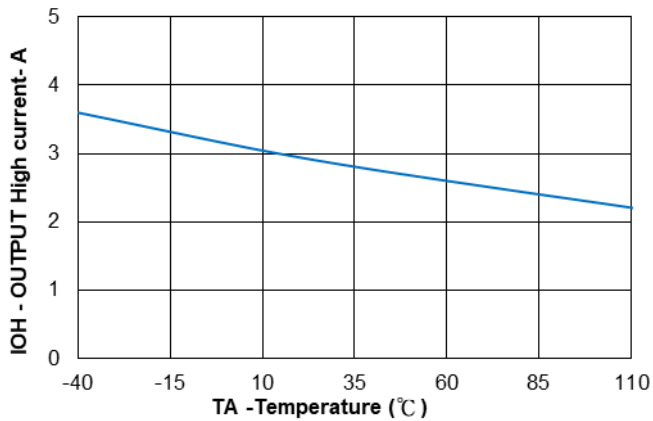


Fig.2 IOL vs. Temperature

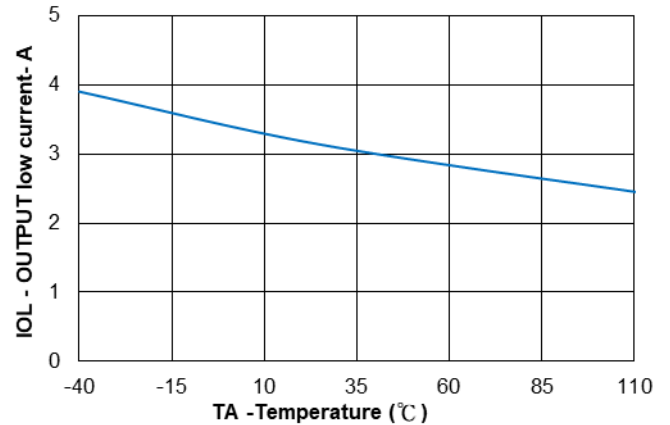


Fig.3 VOH vs. temperature

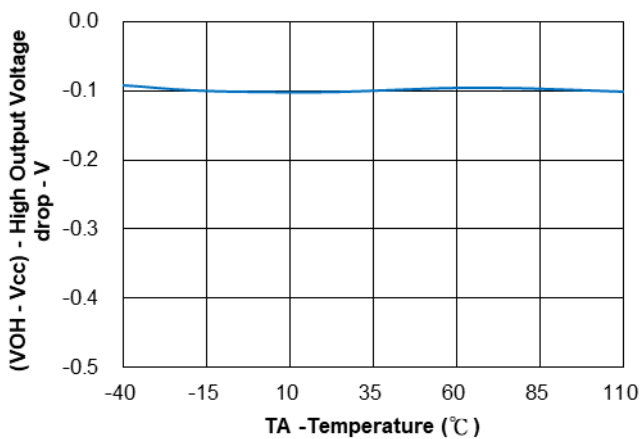


Fig.4 VOL vs. temperature

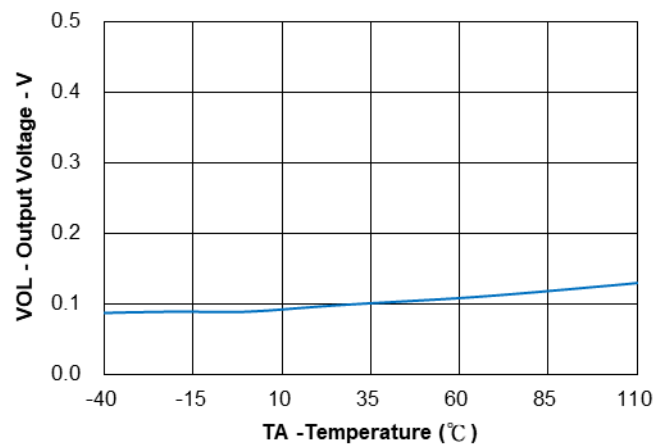


Fig.5 VOH vs. IOH

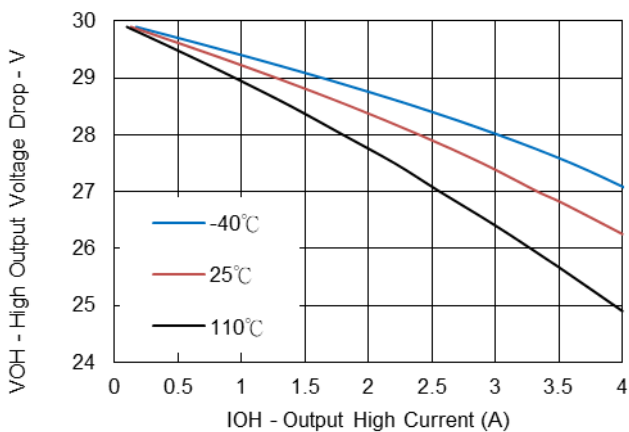


Fig.6 VOL vs. IOL

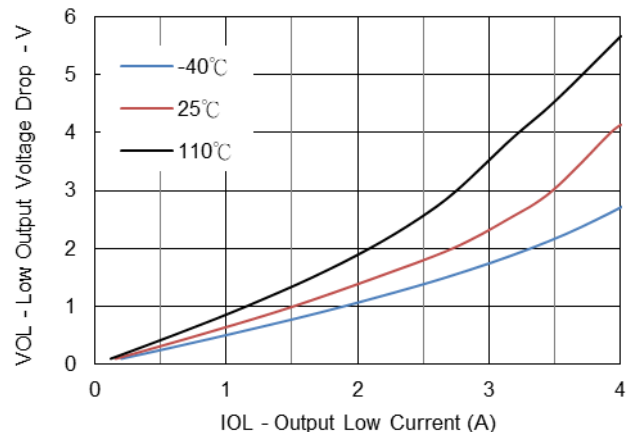


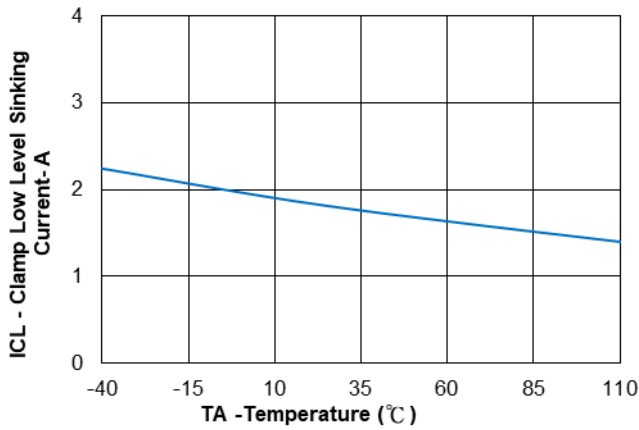
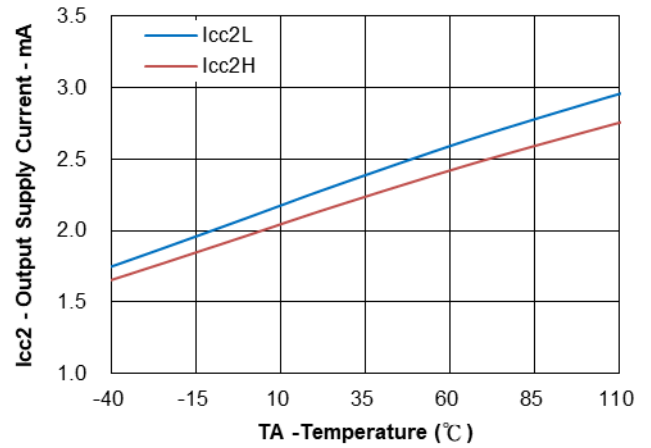
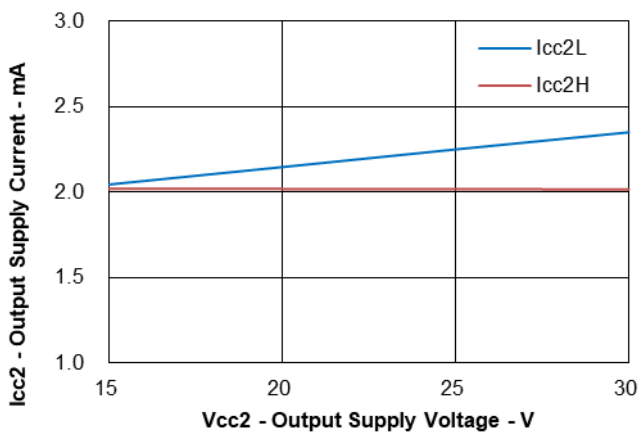
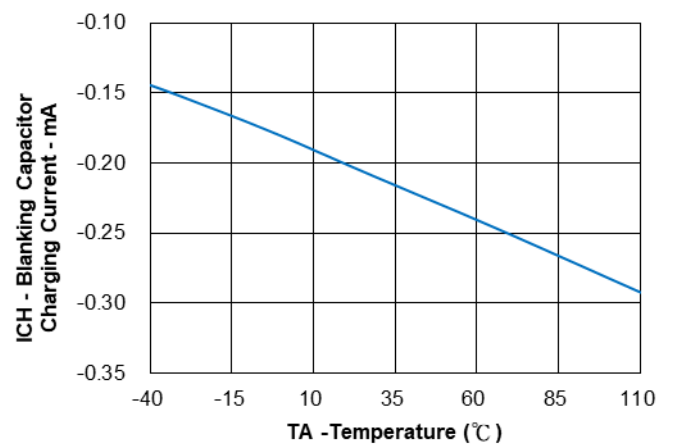
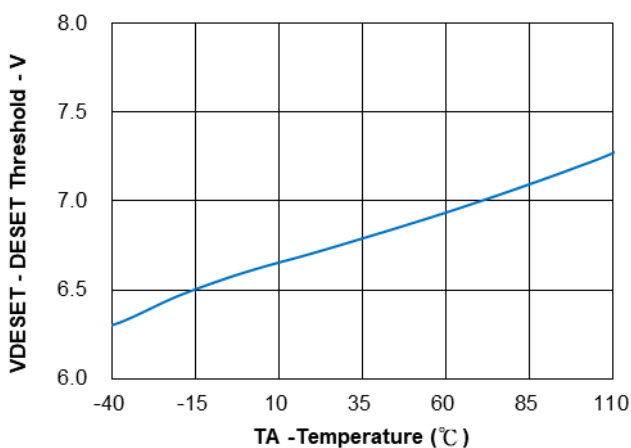
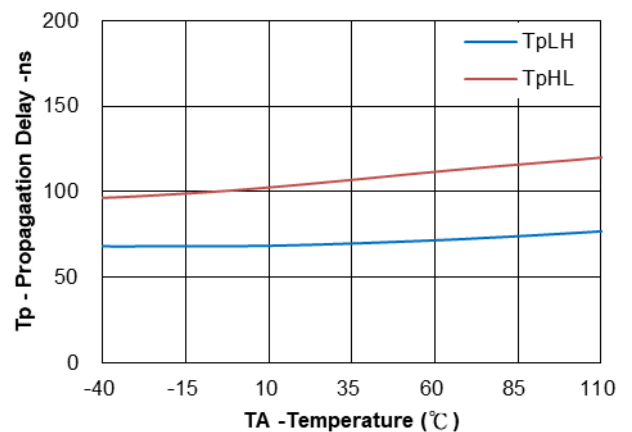
Fig.7 ICL vs. temperature

Fig.8 ICC2 vs. temperature

Fig.9 ICC2 vs. VCC2

Fig.10 ICHG vs. temperature

Fig.11 VDESET threshold vs. temperature

Fig.12 Propagation delay vs. temperature


Fig.13 Propagation delay vs. supply voltage

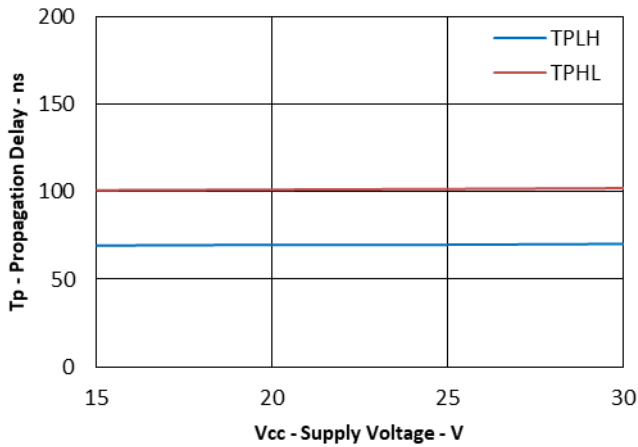


Fig.14 Propagation delay vs. RL

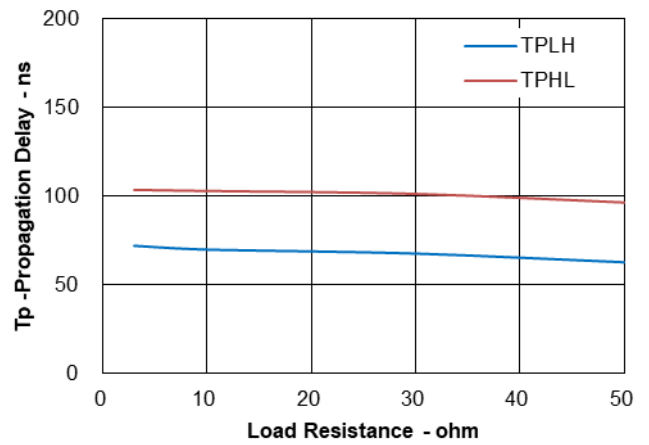


Fig.15 Propagation delay vs. CL

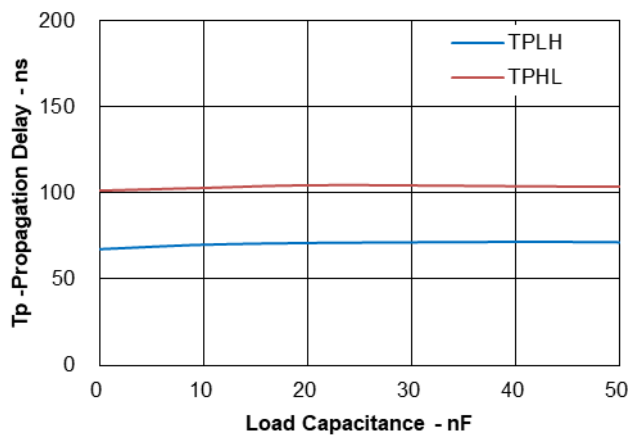


Fig.16 TDESAT90% vs. temperature

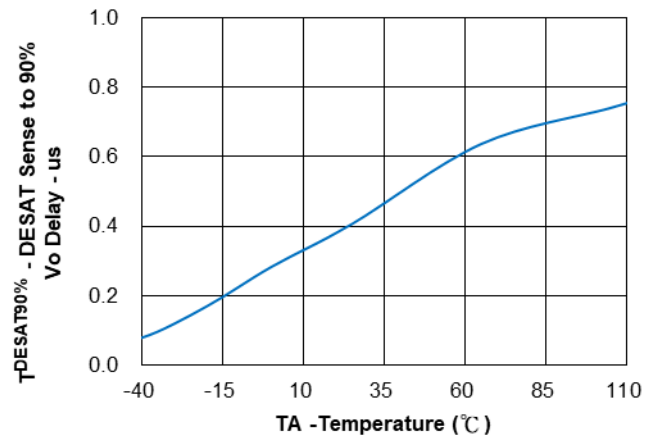


Fig.17 TDESAT10% vs. temperature

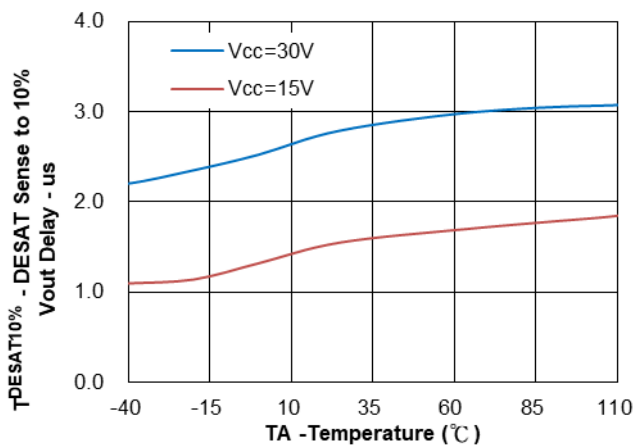


Fig.18 TDESAT10% vs. RL

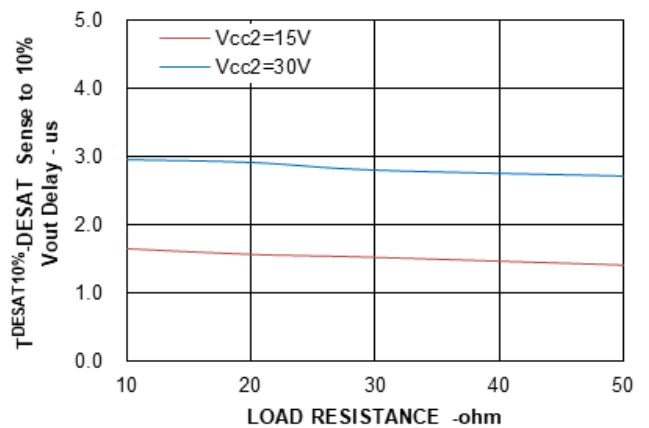


Fig.19 TDESAT10% vs. CL

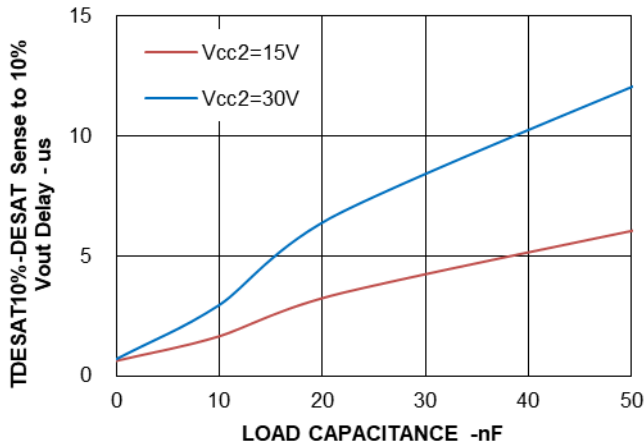


Fig.20 IOH Pulsed test circuit

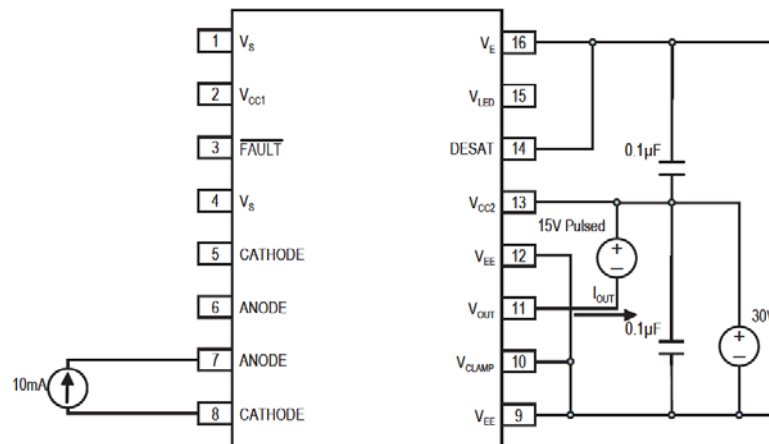


Fig.21 IOL Pulsed test circuit

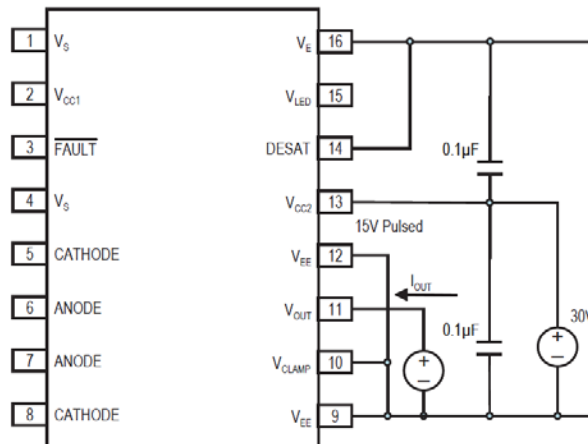


Fig.22 VOH Pulsed test circuit

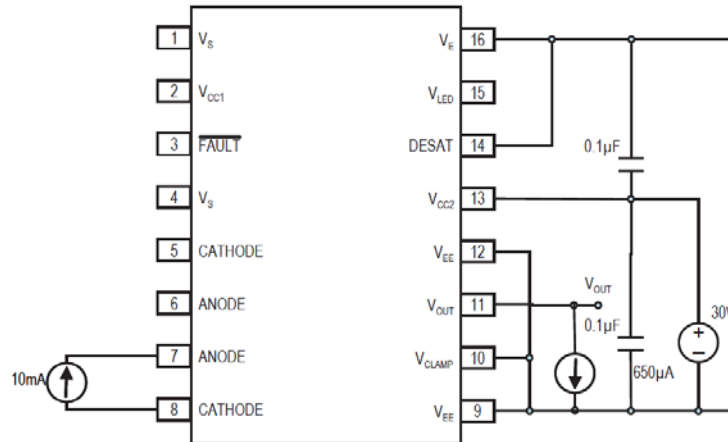


Fig.23 VOL Pulsed test circuit

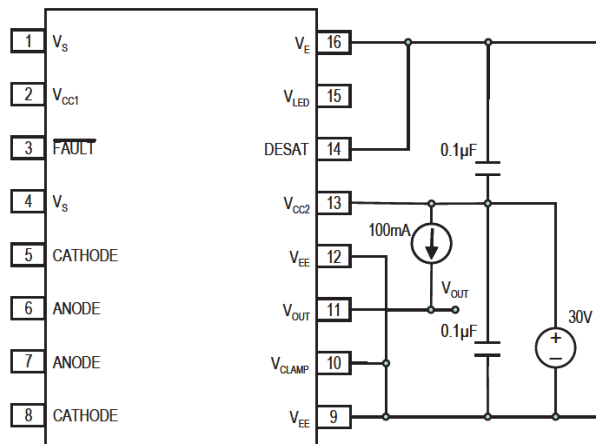


Fig.24 ICC2H test circuit

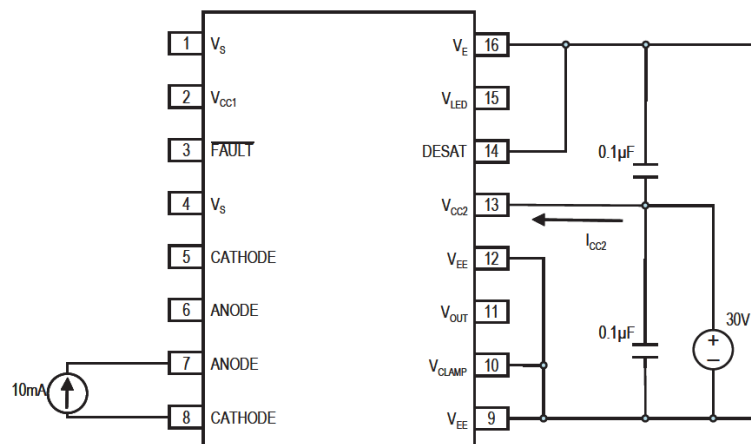


Fig.25 ICC2L test circuit

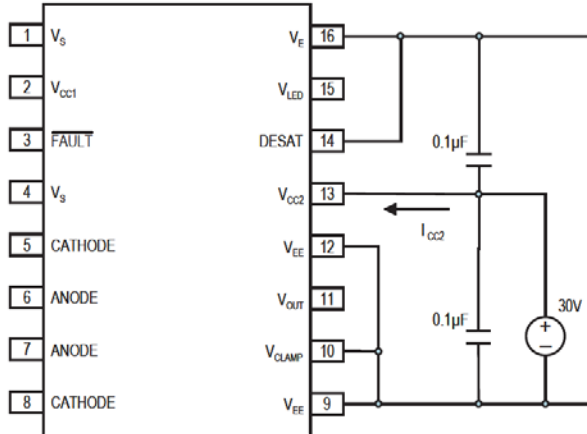


Fig.26 ICHG Pulsed test circuit

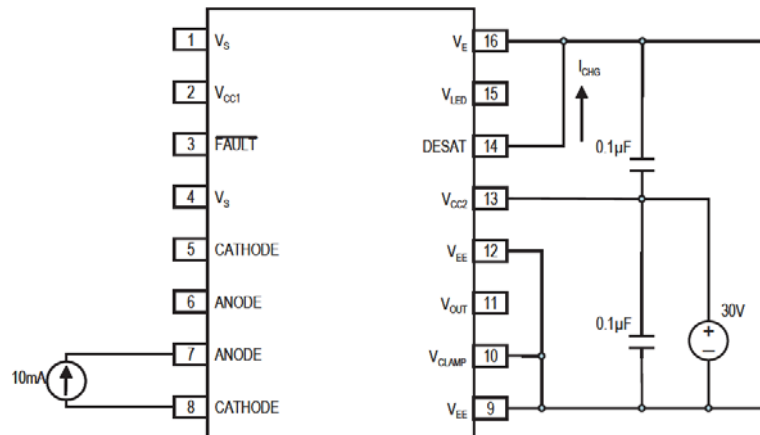


Fig.27 IDSCHG test circuit

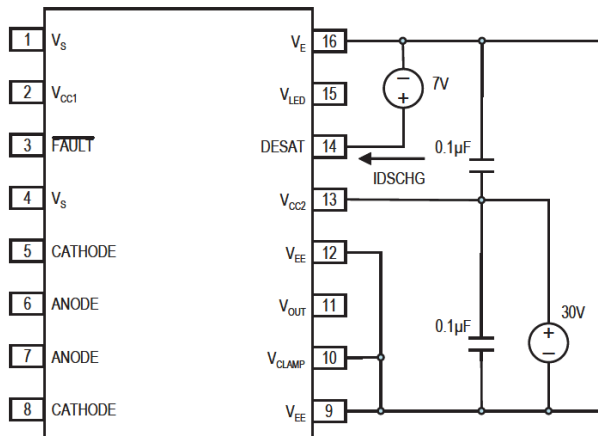


Fig.28 tPLH, tPHL, tf, tr, test circuit

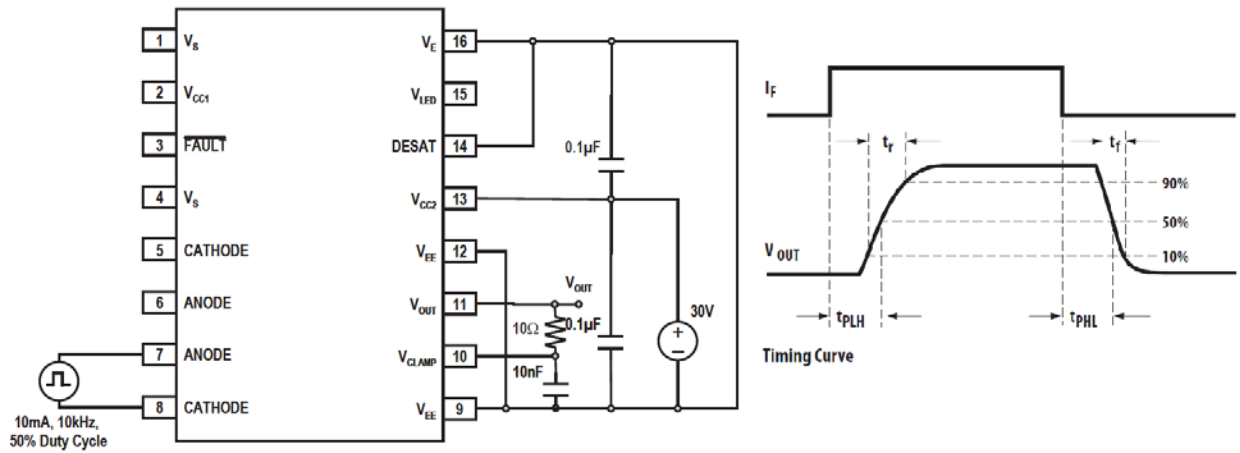
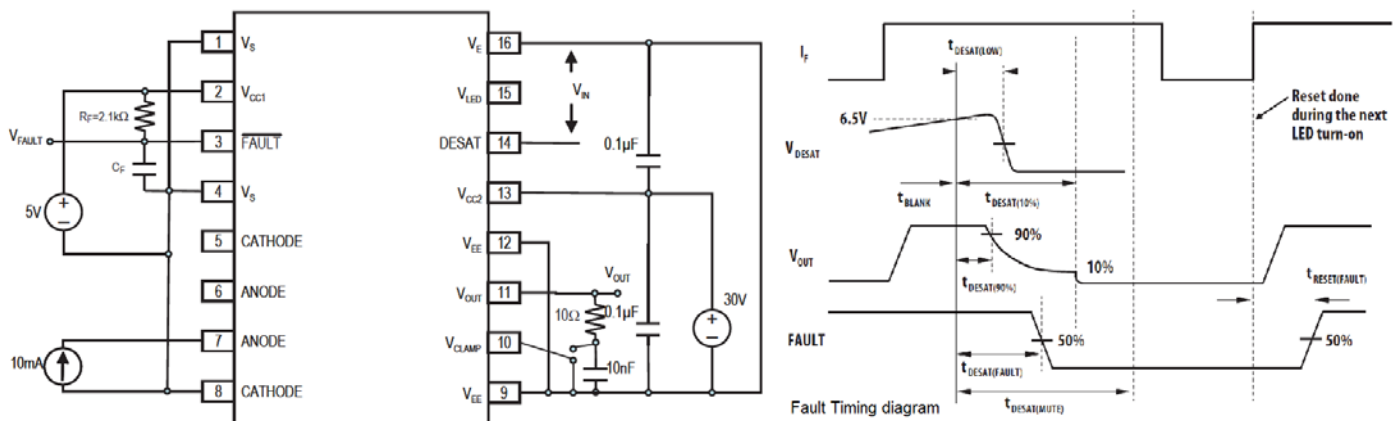


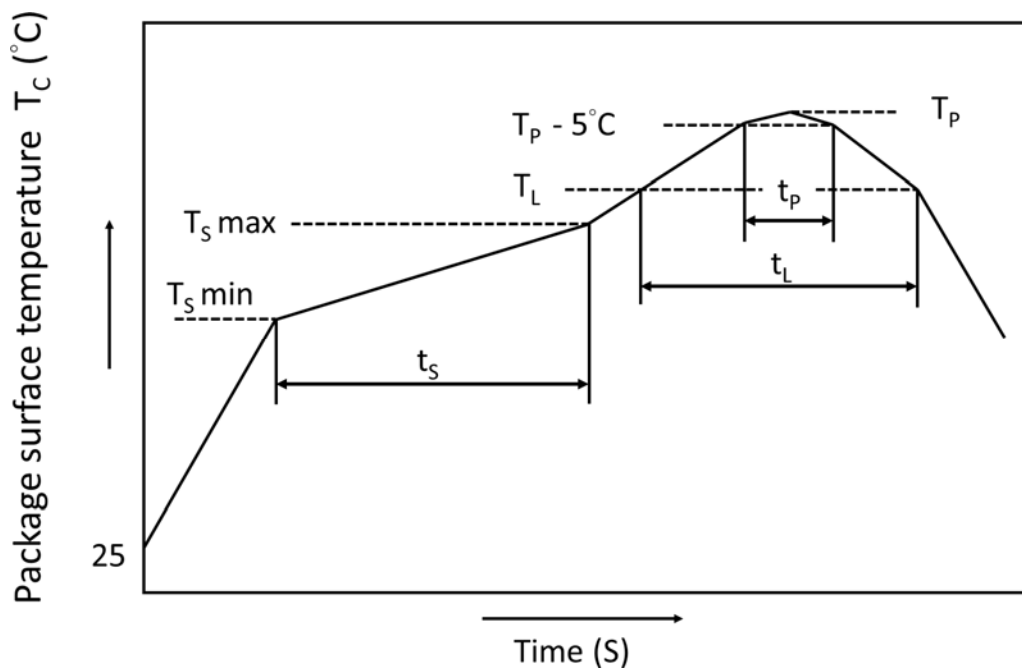
Fig.29 tDESAT fault test circuit



- **Recommended Soldering Conditions**

IR Reflow soldering : One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.

Recommended Temperature Profile of Infrared Reflow



Profile Item	Symbol	Min.	Max.	Unit
Preheat temperature	T_S	150	200	$^\circ\text{C}$
Preheat time	t_s	60	120	s
Ramp-up rate (T_L to T_P)	-	—	3	$^\circ\text{C/s}$
Liquidus temperature	T_L	217		$^\circ\text{C}$
Time above T_L	t_L	60	100	s
Peak Temperature	T_P	—	260	$^\circ\text{C}$
Time during which T_C is between ($T_P - 5$) and T_P	t_p	—	20	s
Ramp-down rate	-	—	6	$^\circ\text{C/s}$

- **Numbering System**

KT5214(Y)-(Z)

Notes:

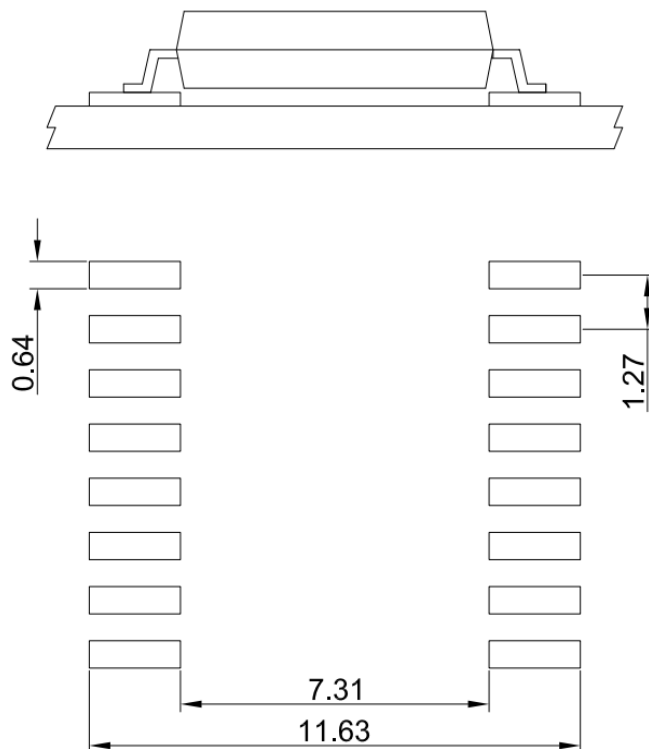
KT5214 = Part No.

Y = Tape and reel option (TLD or TRU)

Z = VDE option (V or None)

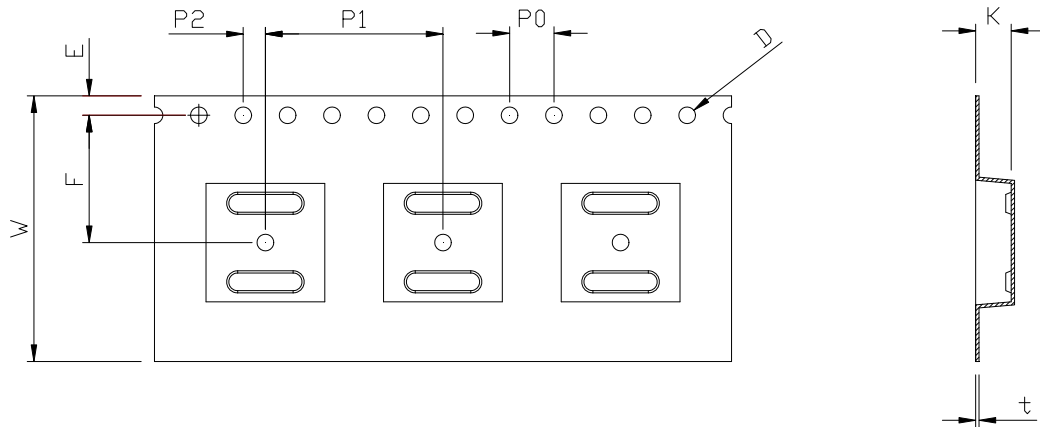
Option	Description	Packing quantity
(TLD)	surface mount type package + TLD tape & reel option	1000 units per reel
(TRU)	surface mount type package + TRU tape & reel option	1000 units per reel

- **Recommended Pad Layout for Surface Mount Lead Form**



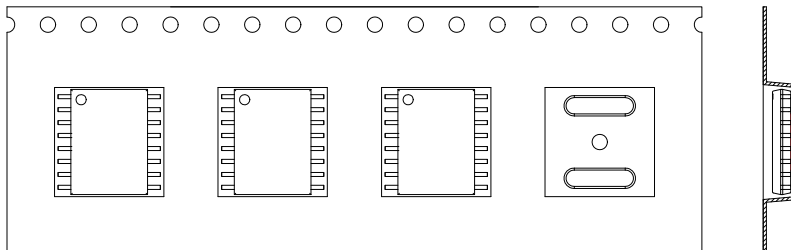
Unit :mm

● **LSOP6 Carrier Tape & Reel**

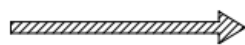
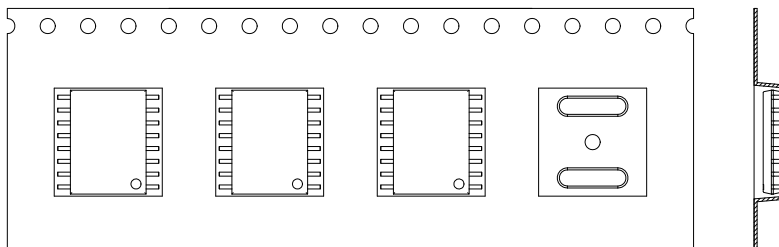


Dimension Symbol	D	E	F	P0	P1	P2	t	W	K
Dimension (mm)	1.5±0.1	1.75±0.1	11.5±0.1	4.0±0.1	16.0±0.1	2.0±0.1	0.3±0.1	24.0±0.3	3.2±0.1

TRU



TLD



Direction of feed from reel

- **Application Notice**

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